GateMate™ FPGA Evaluation Board Datasheet

Evaluation Board Version 3.2 / CCGM1A1 Schematics

DS1003

Datasheet January 2024

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Contents

About this Document

This is a sub-document in an ensemble of GateMate™ FPGA Evaluation Board documents, which include the following documents:

- **DS1003** – GateMate™ FPGA Evaluation Board Datasheet
- **DS1003** – GateMate™ FPGA Evaluation Board Version 3.1 / `CCGM1A1` Schematics

All documents of the evaluation board are always updated together. Please make sure that you use these documents with the same date.

The change history of the complete document ensemble can be found in the main document.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet
- **DS1002** – GateMate™ FPGA Programmer Board Datasheet
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

Chapter 1

Mechanical Dimensions

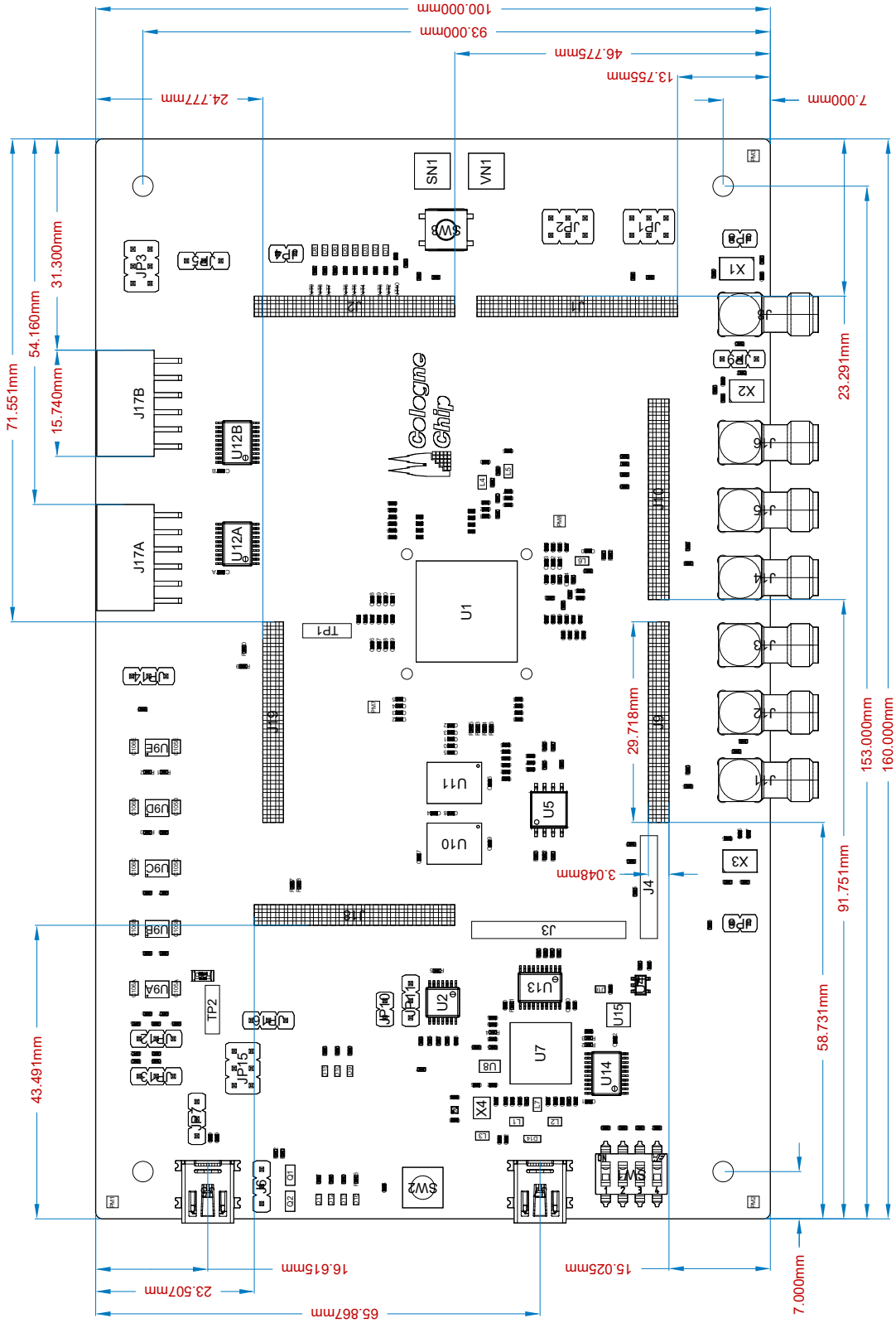


Figure 1.1: *Board dimensions and position of connectors*

Chapter 2

Summary Overviews

2.1 PCB components

Figure 2.1 points out partial circuits that have been described in the previous chapters. The corresponding Table 2.1 lists all associated Figures and where they can be found in this document.

Table 2.1: *Component locations on the GateMate™ FPGA Evaluation Board 3.2A (numbering in counter clockwise order)*

Marking	Function	Shown in Fig.	on Page
1	FPGA core voltage	3.3	22
2	PCB power supply	3.1	21
3	GPIO supply voltage selection (banks WC and NA)	3.4	24
4	Configuration status (LEDs for CFG_DONE and CFG_FAILED_N)	3.12	31
5	Reset	3.10	30
6	HyperRam device	3.18	38
7	USB bridge	3.7	27
8	Flash memory	3.7	27
9	SPI interface	3.7, 3.8	27, 28
10	JTAG interface	3.7, 3.9	27, 28
11	Configuration mode setup	Tab. 3.5	29
12	Power-on reset (POR) enable	3.10	30
13	SerDes LVDS clock	3.14	32
14	SerDes interface	3.19	39
15	GateMate™ FPGA CCGM1A1	1.2	13
16	On-board oscillator CLOCK0_IN	3.13	32
17	Optional clock signals CLOCK1_IN ..CLOCK3_IN	3.15	33
18	GPIO supply voltage selection (banks EA and EB) with alternative LEDs and push button on bank EB	3.4	24
19	Pmod interface	3.17	37

Please note that all references point to the main document **DS1003** – Evaluation Board Datasheet.

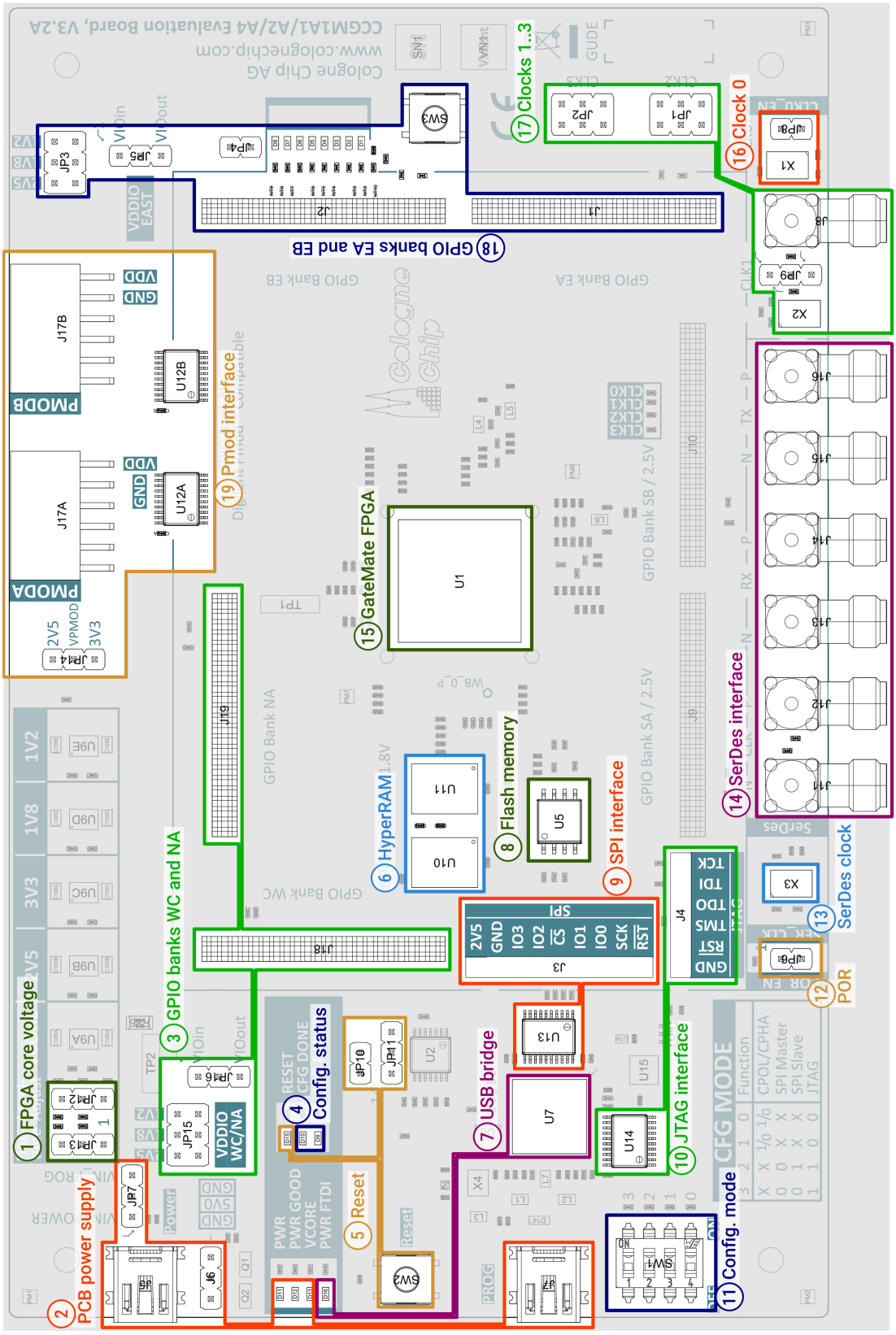


Figure 2.1: *Component locations on the GateMate™ FPGA Evaluation Board 3.2A*

2.2 Default Jumper Settings

Table 2.2: *Default jumper settings*

Designator	Color	Function	Default	Shown in Fig.	on Page
JP1 *	black	Clock distribution from user application to FPGA CLOCK2 signal.	–	3.15	33
JP2 *	black	Clock distribution from user application to FPGA CLOCK3 signal.	–	3.15	33
JP3	blue	Select supply voltage for GPIO banks EA and EB and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.5	25
JP4	black	Enable LEDs on GPIO bank EB.	closed	3.5	25
JP5	blue	Select supply voltage for GPIO banks EA and EB (from JP3 or user application supply output VIOout).	1-2: JP3	3.5	25
JP6	black	Enable power-on reset (POR) module.	closed	3.10	30
JP7	red	Power source selection from J5 or J7.	2-3: J7	3.1	21
JP8	black	Oscillator enable for CLOCK0 signal.	closed	3.13	32
JP9 *	black	CLOCK1 source selection from on-board oscillator * or external source via SMA jack J8 *.	–	3.15	33
JP10	black	Enable reset signal from user application.	opened	3.10	30
JP11	black	Select reset signal input of user application (reset button only or any board reset).	opened	3.10	30
JP12	red	Core voltage level adjustment (low power, economy or speed mode).	1-2: econ.	3.3	22
JP13	red	Core voltage fine tuning (min, typ, max).	1-2: typ	3.3	22
JP14	red	Select Pmod supply voltage 3.3 V or 2.5 V.	1-2: 3.3 V	3.17	37
JP15	blue	Select supply voltage for GPIO banks NA and WC and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.4	24
JP16	blue	Select supply voltage for GPIO banks NA and WC (from JP15 or user application supply output VIOout).	1-2: JP15	3.4	24

* Not populated in its shipped configuration.

Please note that all references point to the main document **DS1003** – evaluation board datasheet.

2.3 LEDs and Push Buttons

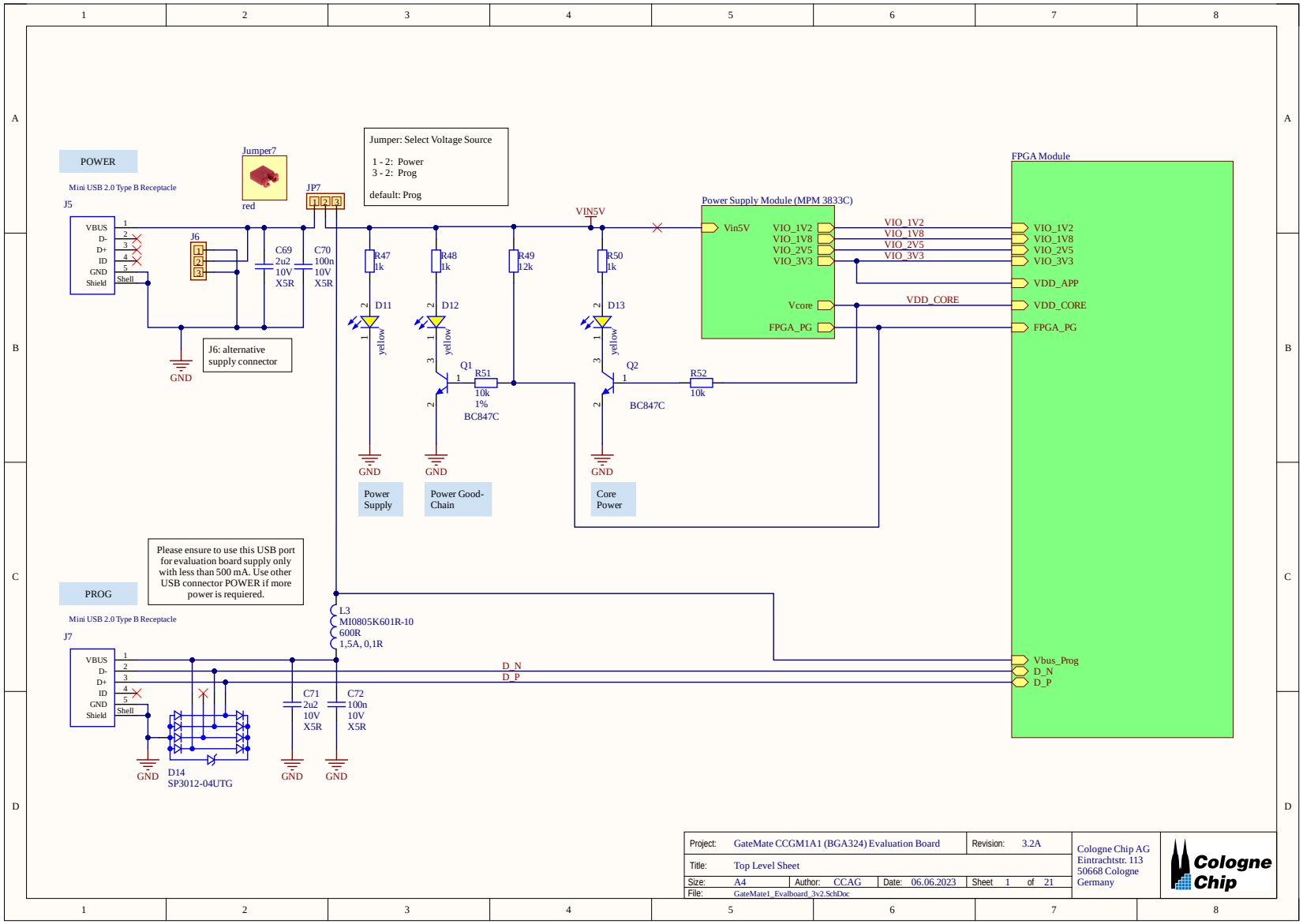
Table 2.3: *LEDs and push buttons*

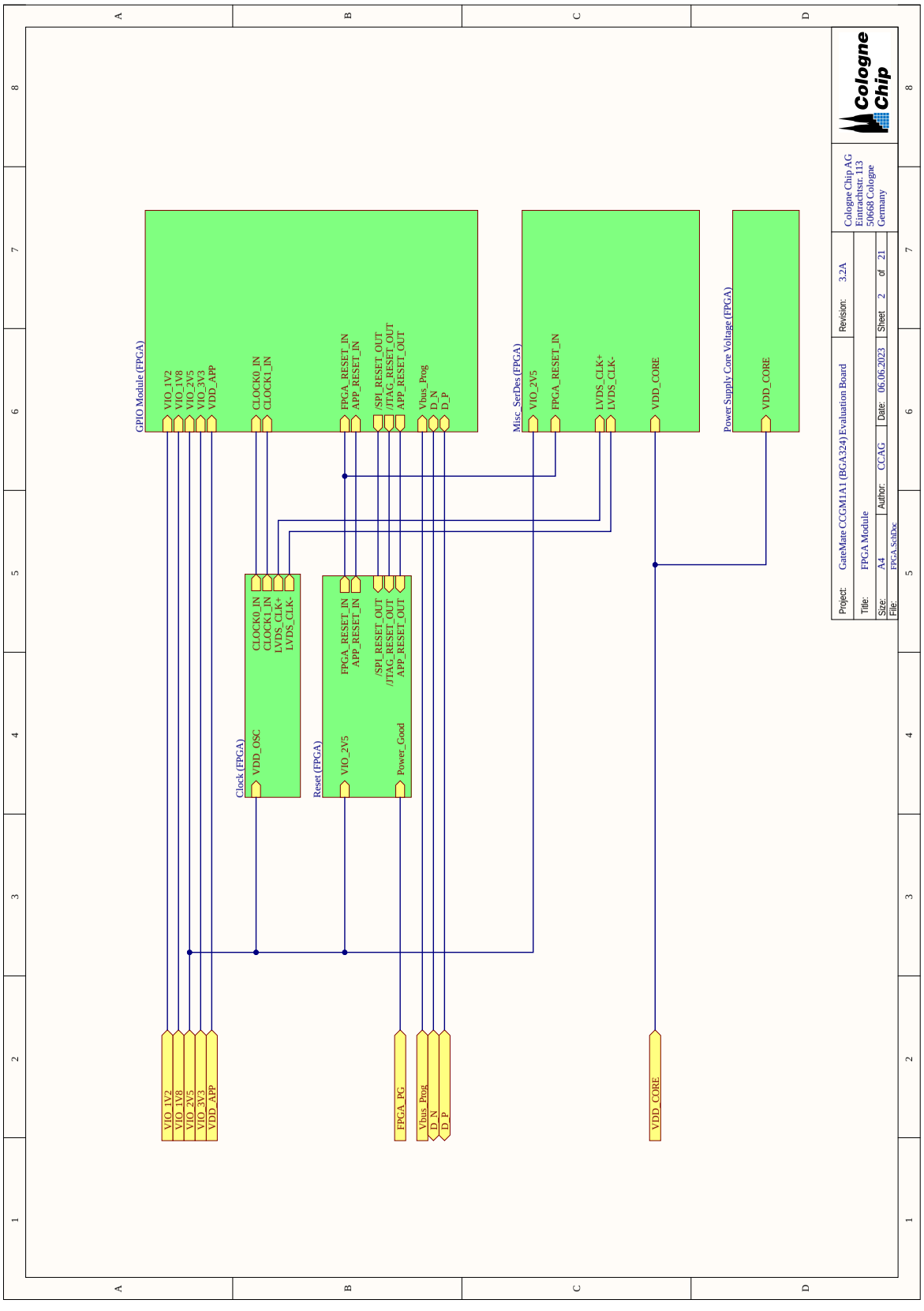
Designator	Color	Function	Shown in Fig.	on Page
D1 . . D8	green	User LEDs assigned to GPIO bank EB	3.5	25
D9	red	Configuration state CFG_FAILED_N	3.12	31
D10	green	Configuration state CFG_DONE	3.12	31
D11	yellow	PCB power supply	3.1	21
D12	yellow	Power good notification from on-board DC-DC converters	3.1	21
D13	yellow	FPGA core power	3.1	21
D15	red	FPGA reset	3.10	30
D16	yellow	Power supply from USB data jack J7 (supply for U7, FT2232HQ-Reel)	2.1, 3.7	15, 27
SW2	red	PCB reset	3.10	30
SW3	black	User button assigned to GPIO bank EB	3.5	25

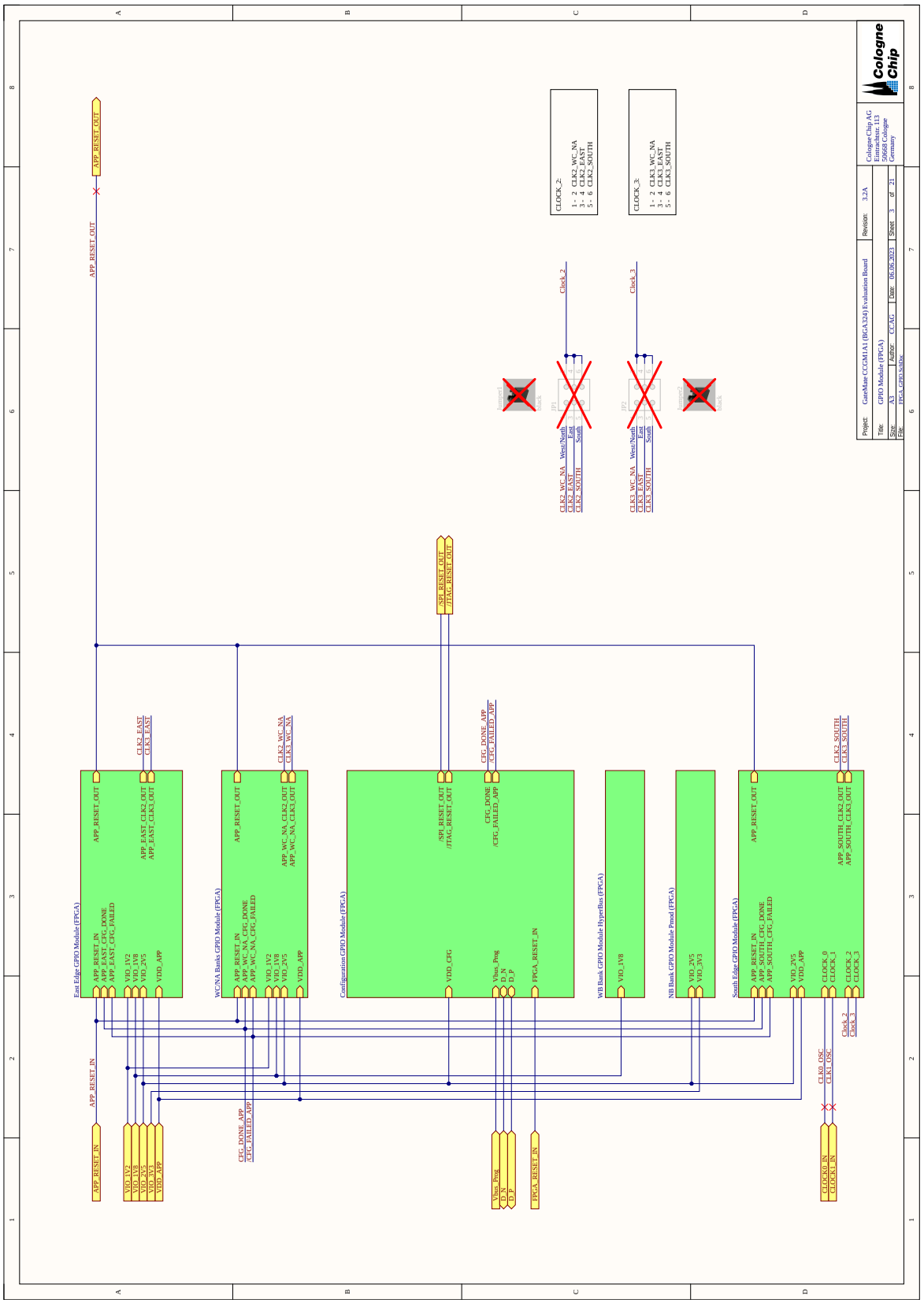
Please note that all references point to the main document **DS1003** – Evaluation Board Datasheet.

Chapter 3

Evaluation Board Schematics


POWER
Mini USB 2.0 Type B Receptacle
J5
VBUS
D-
D+
ID
GND
Shell
Jumper7
red
JP7
J6
C69
2u2
10V
X5R
C70
100n
10V
X5R
GND
J6: alternative supply connector
Jumper: Select Voltage Source
1 - 2: Power
3 - 2: Prog
default: Prog
VIN5V
R47
1k
R48
1k
R49
12k
R50
1k
D11
D12
D13
yellow
Q1
Q2
R51
10k
1%
BC847C
R52
10k
Power Supply
Power Good-Chain
Core Power
Power Supply Module (MPM 3833C)
Vin5V
VIO_1V2
VIO_1V8
VIO_2V5
VIO_3V3
Vcore
FPGA_PG
VDD_CORE
FPGA Module
VDD_APP
PROG
Please ensure to use this USB port for evaluation board supply only with less than 500 mA. Use other USB connector POWER if more power is requiered.
L3
MI0805K601R-10
600R
1,5A, 0,1R
J7
D_N
D_P
Vbus_Prog
C71
2u2
10V
X5R
C72
100n
10V
X5R
D14
SP3012-04UTG
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Top Level Sheet
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 1 of 21
File: GateMate1_Evalboard_3v2.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


GPIO Module (FPGA)
VIO_1V2
VIO_1V8
VIO_2V5
VIO_3V3
VDD_APP
CLOCK0_IN
CLOCK1_IN
FPGA_RESET_IN
APP_RESET_IN
/SPI_RESET_OUT
/JTAG_RESET_OUT
APP_RESET_OUT
Vbus_Prog
D_N
D_P
Misc_SerDes (FPGA)
VIO_2V5
FPGA_RESET_IN
LVDS_CLK+
LVDS_CLK-
VDD_CORE
Power Supply Core Voltage (FPGA)
VDD_CORE
Clock (FPGA)
VDD_OSC
Reset (FPGA)
VIO_2V5
Power_Good
FPGA_PG
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: FPGA Module
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 2 of 21
File: FPGA.SchDoc


Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: GPIO Module (FPGA)
Size: A3
Author: CC-AG
Date: 06.06.2023
Sheet 3 of 21
File: FPGA_GPIO.SchDoc
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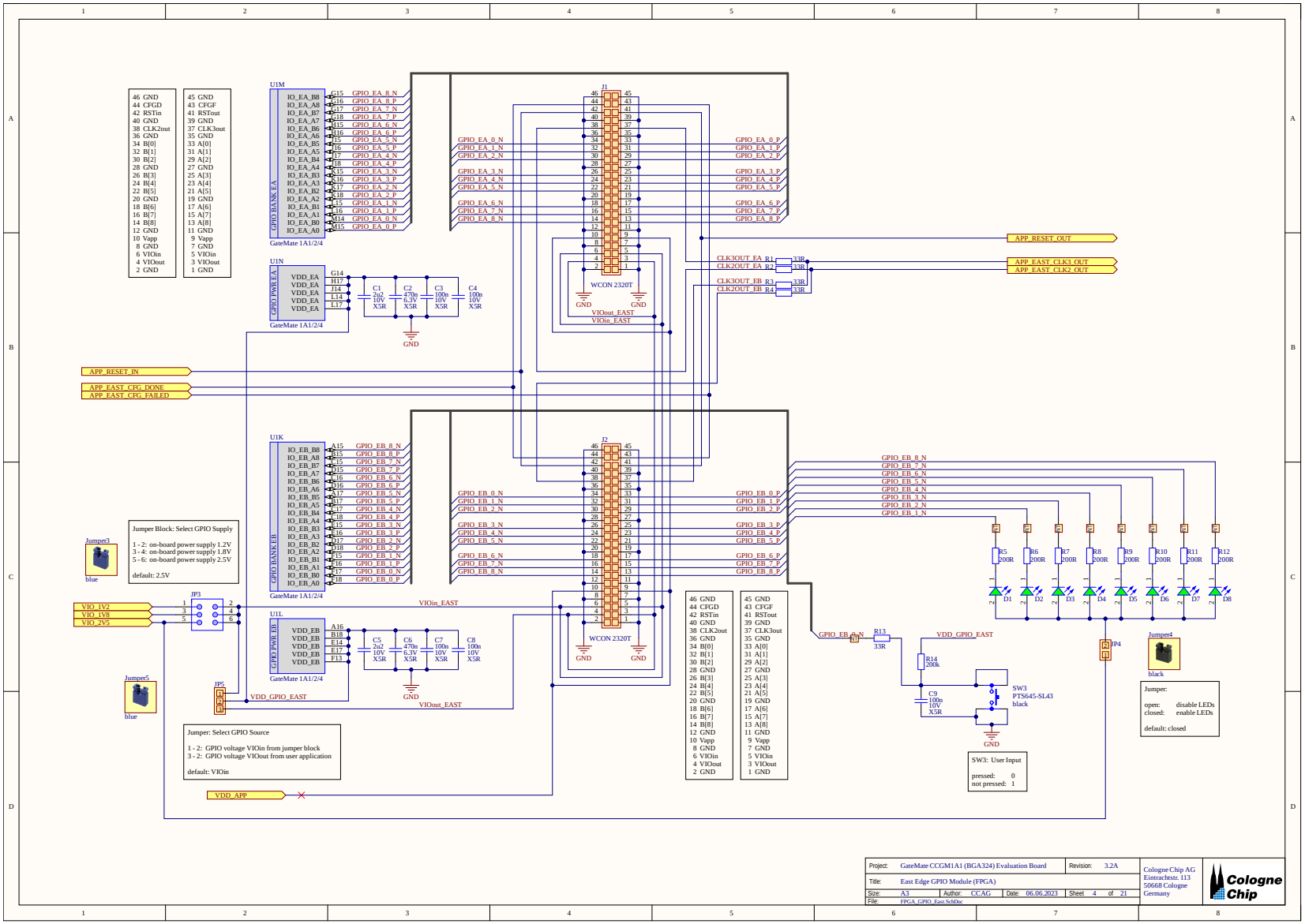
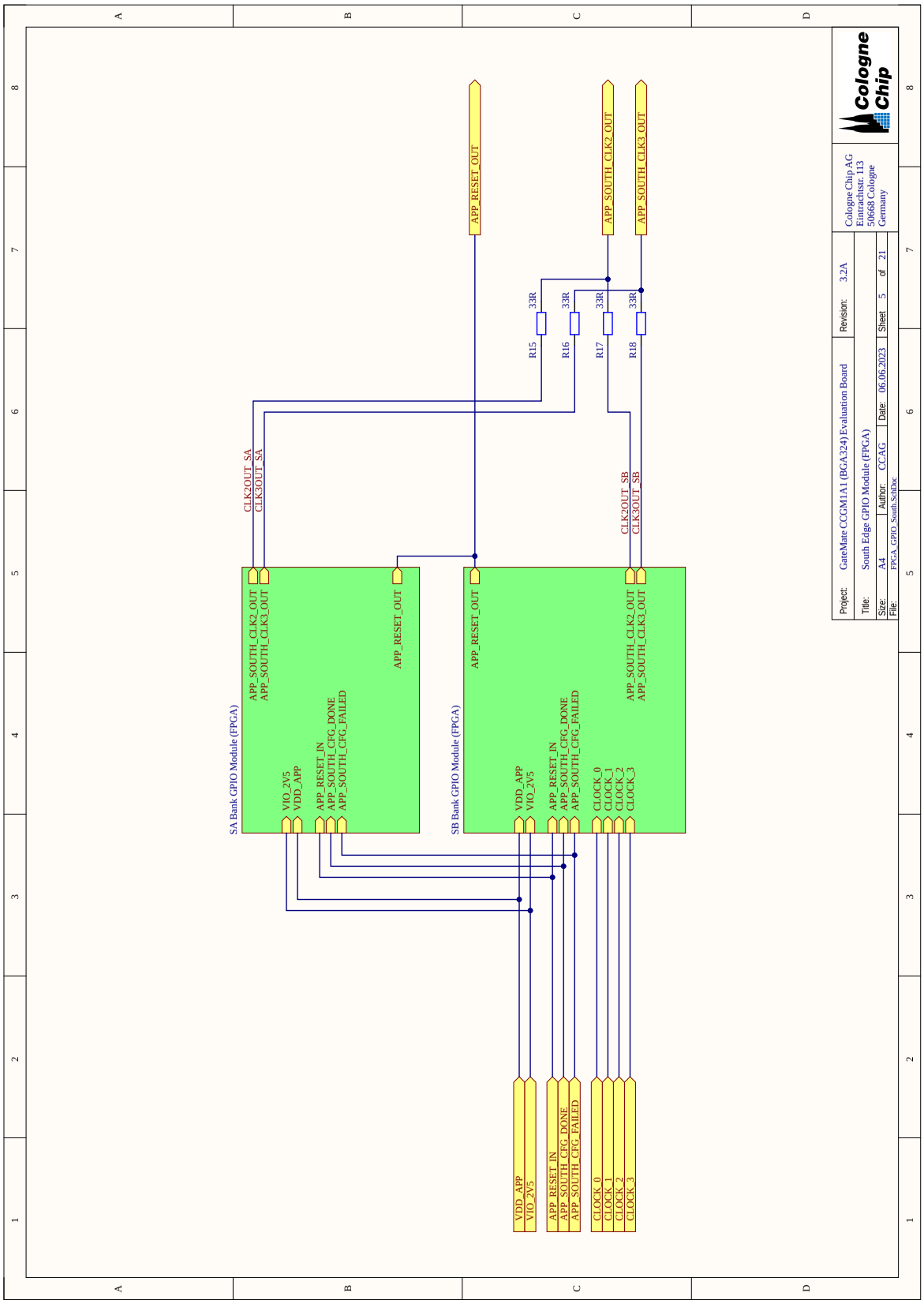
Germany
East Edge GPIO Module (FPGA)
WC/NA Banks GPIO Module (FPGA)
Configuration GPIO Module (FPGA)
WB Bank GPIO Module HyperBus (FPGA)
NB Bank GPIO Module Pmod (FPGA)
South Edge GPIO Module (FPGA)
APP_RESET_OUT
APP_RESET_IN
CLOCK_2:
CLOCK_3:
CLK2_WC_NA
CLK2_EAST
CLK2_SOUTH
CLK3_WC_NA
CLK3_EAST
CLK3_SOUTH
SPI_RESET_OUT
JTAG_RESET_OUT
CFG_DONE_APP
CFG_FAILED_APP
FPGA_RESET_IN
CLK0_OSC
CLK1_OSC
CLOCK0_IN
CLOCK1_IN
Clock_2
Clock_3
VDD_1V2
VDD_1V8
VDD_2V5
VDD_3V3
VDD_APP


U1M
U1N
U1K
U1L
J1
J2
GateMate 1A1/2/4
WCON 2320T
APP_RESET_IN
APP_EAST_CFG_DONE
APP_EAST_CFG_FAILED
APP_RESET_OUT
APP_EAST_CLK3_OUT
APP_EAST_CLK2_OUT
VIO_1V2
VIO_1V8
VIO_2V5
VIOin_EAST
VIOout_EAST
VDD_GPIO_EAST
VDD_APP
Jumper3
Jumper4
Jumper5
JP3
JP4
JP5
Jumper Block: Select GPIO Supply
1 - 2: on-board power supply 1.2V
3 - 4: on-board power supply 1.8V
5 - 6: on-board power supply 2.5V
default: 2.5V
Jumper: Select GPIO Source
1 - 2: GPIO voltage VIOin from jumper block
3 - 2: GPIO voltage VIOout from user application
default: VIOin
Jumper:
open: disable LEDs
closed: enable LEDs
default: closed
SW3: User Input
pressed: 0
not pressed: 1
SW3 PTS645-SL43 black
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: East Edge GPIO Module (FPGA)
Size: A3
Author: CCAG
Date: 06.06.2023
Sheet 4 of 21
File: FPGA_GPIO_East.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


APP_RESET_OUT
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
R15 33R
R16 33R
R17 33R
R18 33R
CLK2OUT_SA
CLK3OUT_SA
CLK2OUT_SB
CLK3OUT_SB
SA Bank GPIO Module (FPGA)
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
APP_RESET_OUT
VIO_2V5
VDD_APP
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
SB Bank GPIO Module (FPGA)
APP_RESET_OUT
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
VDD_APP
VIO_2V5
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
VDD_APP
VIO_2V5
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: South Edge GPIO Module (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 5 of 21
File: FPGA_GPIO_South.SchDoc
Cologne Chip AG
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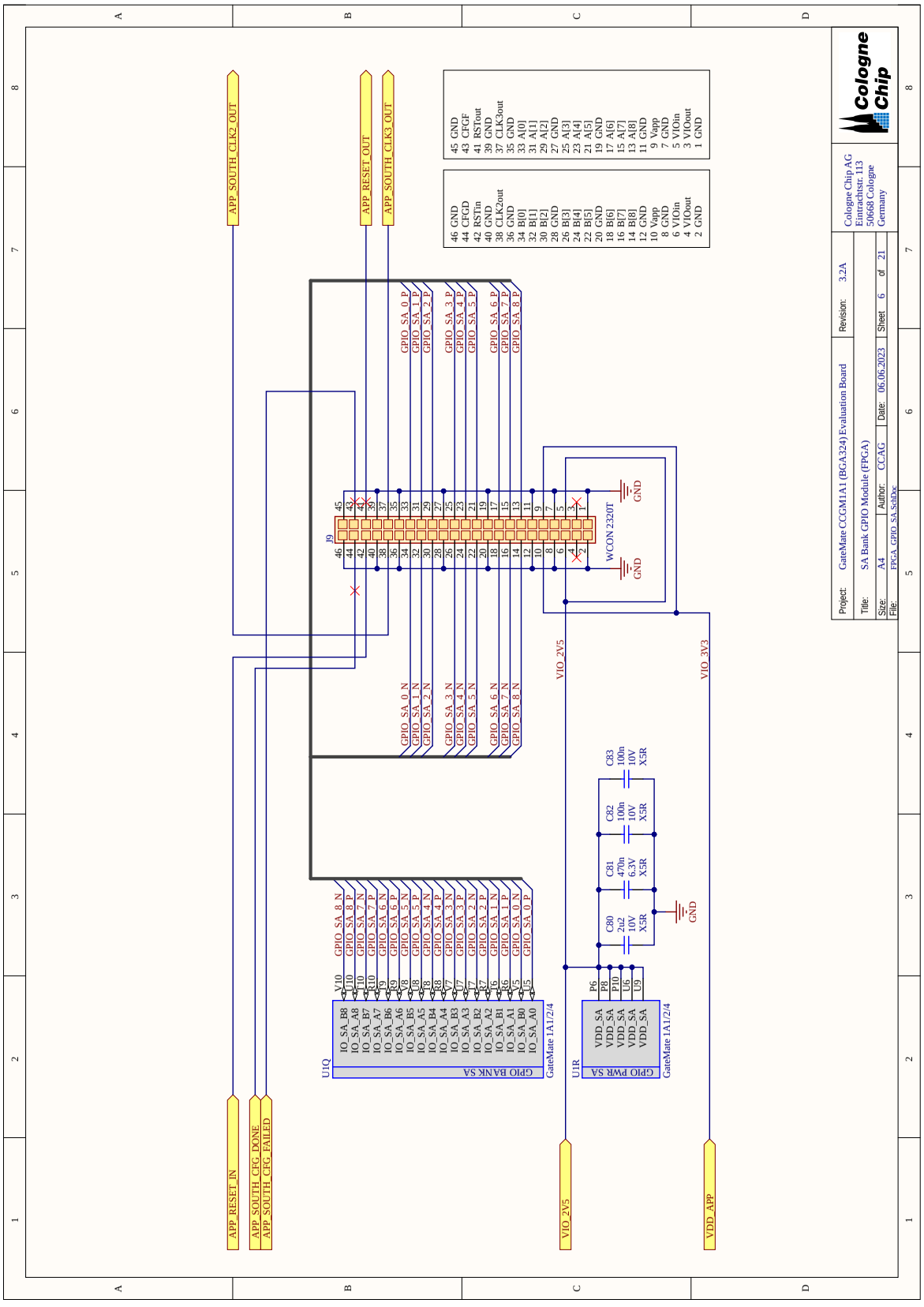
50668 Cologne
Germany


APP_SOUTH_CLK2_OUT
APP_RESET_OUT
APP_SOUTH_CLK3_OUT
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
VIO_2V5
VIO_3V3
VDD_APP
J9
WCON 2320T
GND
U1Q
GPIO BANK SA
GateMate 1A1/2/4
U1R
GPIO PWR SA
C80 2u2 10V X5R
C81 470n 6.3V X5R
C82 100n 10V X5R
C83 100n 10V X5R
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: SA Bank GPIO Module (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 6 of 21
File: FPGA_GPIO_SA.SchDoc
Cologne Chip AG
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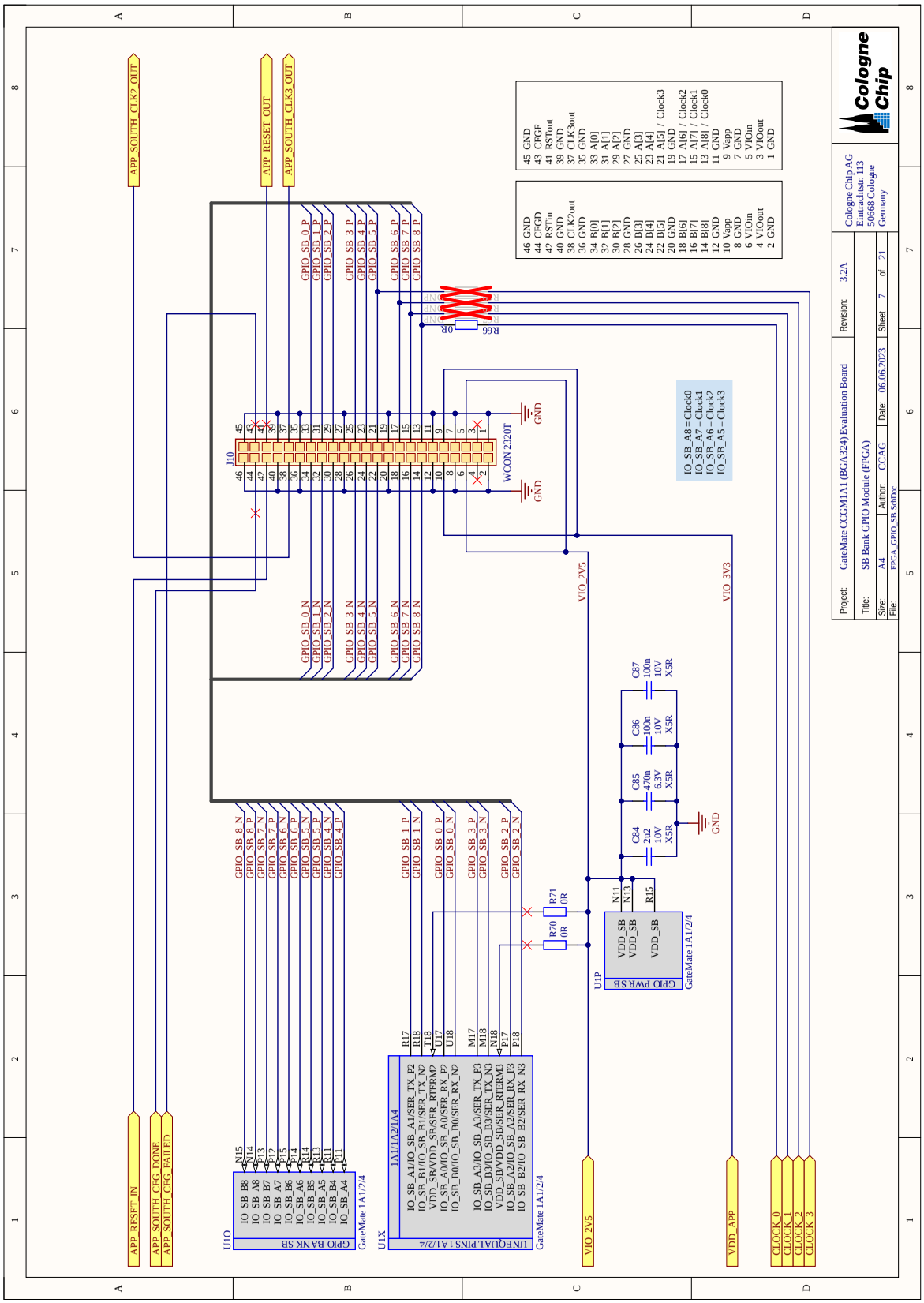
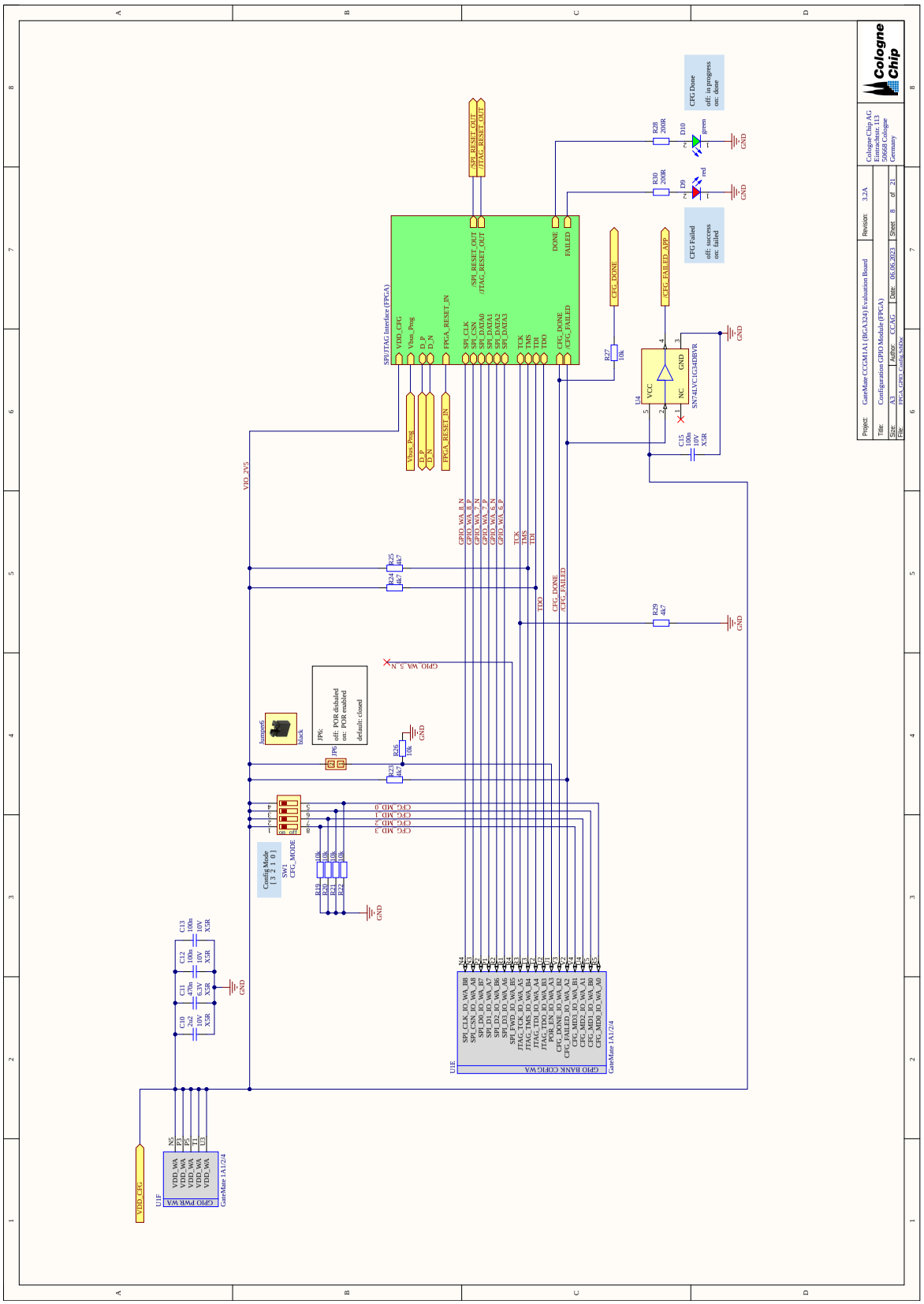
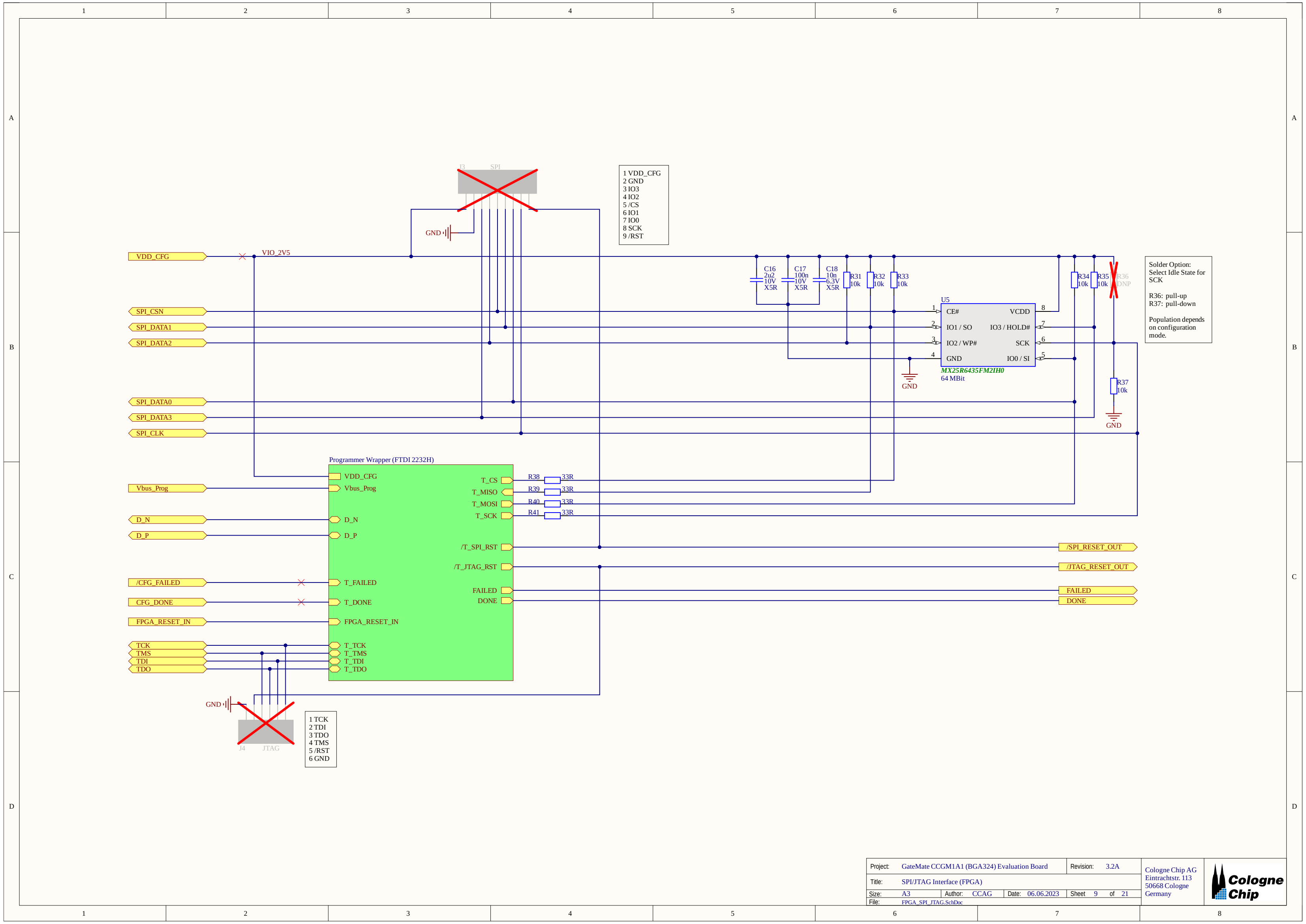
50668 Cologne
Germany


APP_SOUTH_CLK2_OUT
APP_RESET_OUT
APP_SOUTH_CLK3_OUT
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
VDD_APP
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
VIO_2V5
VIO_3V3
J10
WCON 2320T
R66
0R
R70
R71
C84
2u2
C85
470n
C86
100n
C87
100n
U1O
GPIO BANK SB
GateMate 1A1/2/4
U1X
CNFGUAL PINS 1A1/2/4
U1P
GPIO PWR SB
IO_SB_A8 = Clock0
IO_SB_A7 = Clock1
IO_SB_A6 = Clock2
IO_SB_A5 = Clock3
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: SB Bank GPIO Module (FPGA)
Author: CCAG
Date: 06.06.2023
Sheet 7 of 21
Size: A4
File: FPGA_GPIO_SB.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany




VDD_CFG
VIO_2V5
SPI_CSN
SPI_DATA1
SPI_DATA2
SPI_DATA0
SPI_DATA3
SPI_CLK
J3 SPI
GND
1 VDD_CFG
2 GND
3 IO3
4 IO2
5 /CS
6 IO1
7 IO0
8 SCK
9 /RST
C16 2u2 10V X5R
C17 100n 10V X5R
C18 10n 6.3V X5R
R31 10k
R32 10k
R33 10k
R34 10k
R35 10k
R36 DNP
R37 10k
U5
CE#
IO1 / SO
IO2 / WP#
GND
VCDD
IO3 / HOLD#
SCK
IO0 / SI
MX25R6435FM2IH0
64 MBit
Solder Option:
Select Idle State for SCK
R36: pull-up
R37: pull-down
Population depends on configuration mode.
Programmer Wrapper (FTDI 2232H)
VDD_CFG
Vbus_Prog
D_N
D_P
T_FAILED
T_DONE
FPGA_RESET_IN
T_TCK
T_TMS
T_TDI
T_TDO
T_CS
T_MISO
T_MOSI
T_SCK
/T_SPI_RST
/T_JTAG_RST
FAILED
DONE
R38 33R
R39 33R
R40 33R
R41 33R
/SPI_RESET_OUT
/JTAG_RESET_OUT
/CFG_FAILED
CFG_DONE
TCK
TMS
TDI
TDO
J4 JTAG
1 TCK
2 TDI
3 TDO
4 TMS
5 /RST
6 GND
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: SPI/JTAG Interface (FPGA)
Size: A3
Author: CCAG
Date: 06.06.2023
Sheet 9 of 21
File: FPGA_SPI_JTAG.SchDoc
Cologne Chip AG
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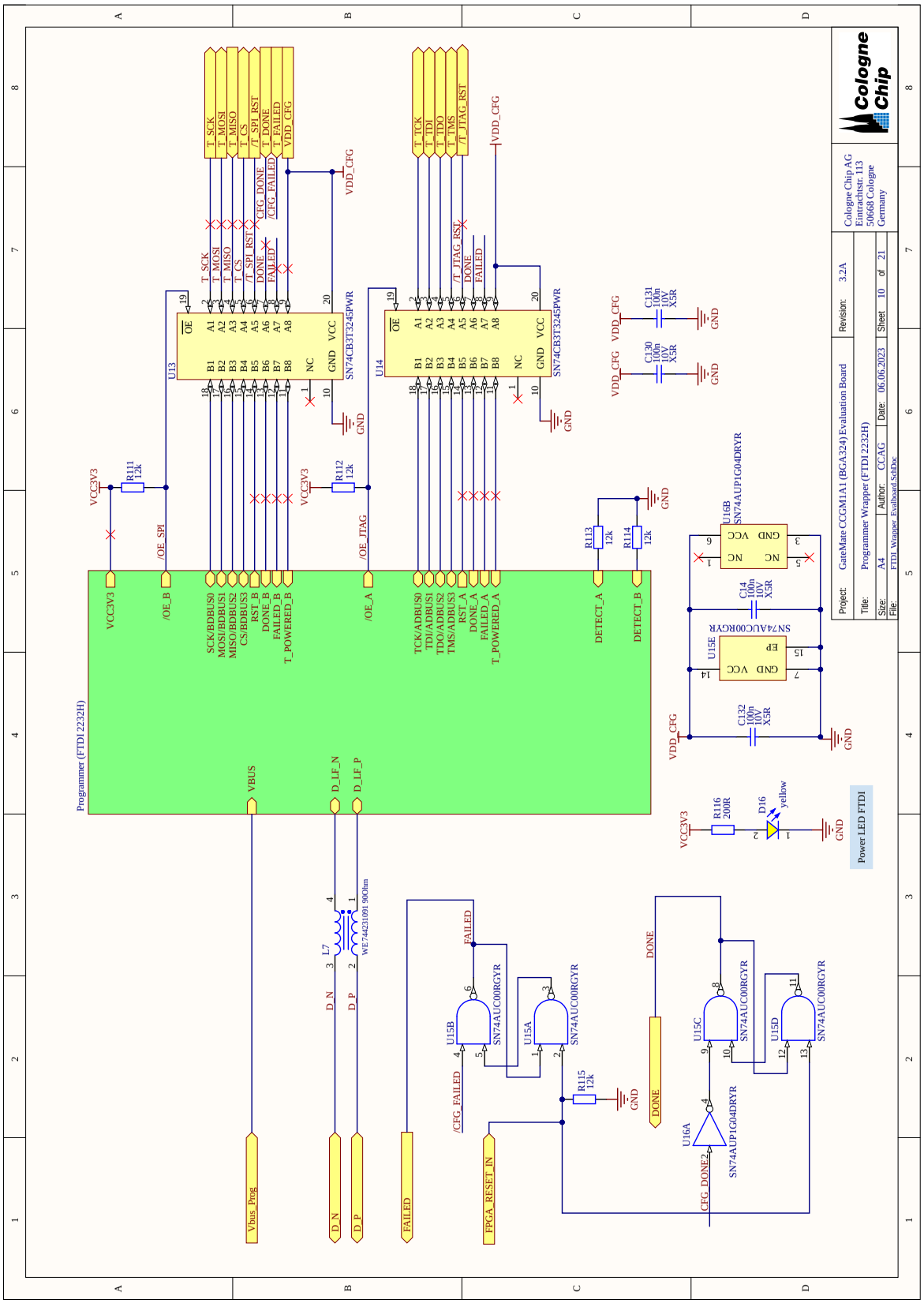
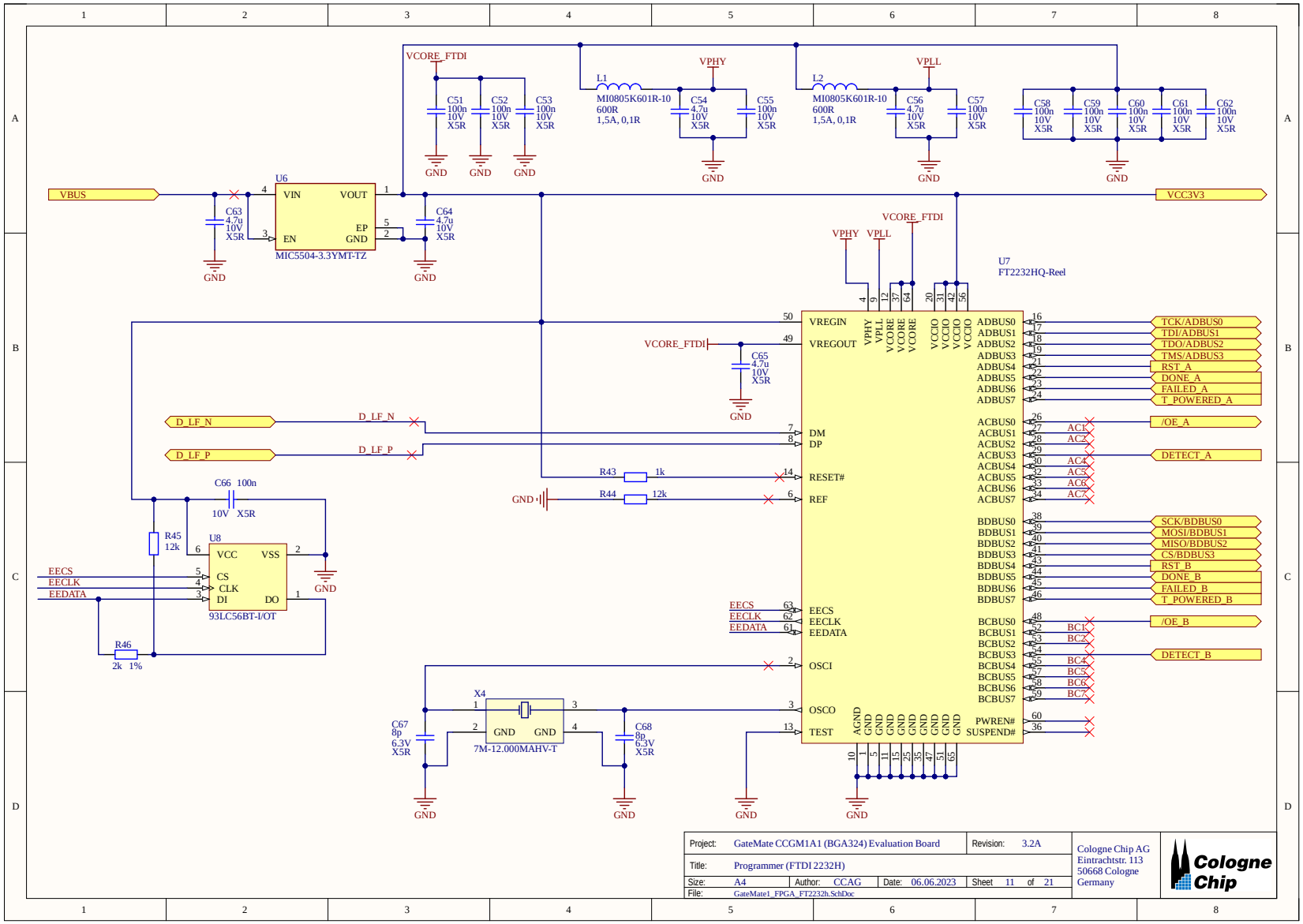
50668 Cologne
Germany
Cologne Chip


Programmer (FTDI 2232H)
SN74CB3T3245PWR
SN74AUP1G04DRYR
SN74AUC00RGYR
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Programmer Wrapper (FTDI 2232H)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 10 of 21
File: FTDI_Wrapper_Evalboard.SchDoc
Power LED FTDI


VCORE_FTDI
VPHY
VPLL
L1
MI0805K601R-10
600R
1,5A, 0,1R
L2
MI0805K601R-10
600R
1,5A, 0,1R
C51 100n 10V X5R
C52 100n 10V X5R
C53 100n 10V X5R
C54 4.7u 10V X5R
C55 100n 10V X5R
C56 4.7u 10V X5R
C57 100n 10V X5R
C58 100n 10V X5R
C59 100n 10V X5R
C60 100n 10V X5R
C61 100n 10V X5R
C62 100n 10V X5R
GND
VBUS
VCC3V3
U6
VIN
VOUT
EN
EP GND
MIC5504-3.3YMT-TZ
C63 4.7u 10V X5R
C64 4.7u 10V X5R
U7
FT2232HQ-Reel
VREGIN
VREGOUT
C65 4.7u 10V X5R
D_LF_N
D_LF_P
DM
DP
R43 1k
R44 12k
RESET#
REF
C66 100n 10V X5R
R45 12k
U8
VCC
VSS
CS
CLK
DI
DO
93LC56BT-I/OT
EECS
EECLK
EEDATA
R46 2k 1%
X4
7M-12.000MAHV-T
C67 8p 6.3V X5R
C68 8p 6.3V X5R
OSCI
OSCO
TEST
PWREN#
SUSPEND#
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
TCK/ADBUS0
TDI/ADBUS1
TDO/ADBUS2
TMS/ADBUS3
RST_A
DONE_A
FAILED_A
T_POWERED_A
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
/OE_A
DETECT_A
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
SCK/BDBUS0
MOSI/BDBUS1
MISO/BDBUS2
CS/BDBUS3
RST_B
DONE_B
FAILED_B
T_POWERED_B
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
/OE_B
DETECT_B
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Programmer (FTDI 2232H)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 11 of 21
File: GateMate1_FPGA_FT2232h.SchDoc
Cologne Chip AG
Eintrachtstr. 113
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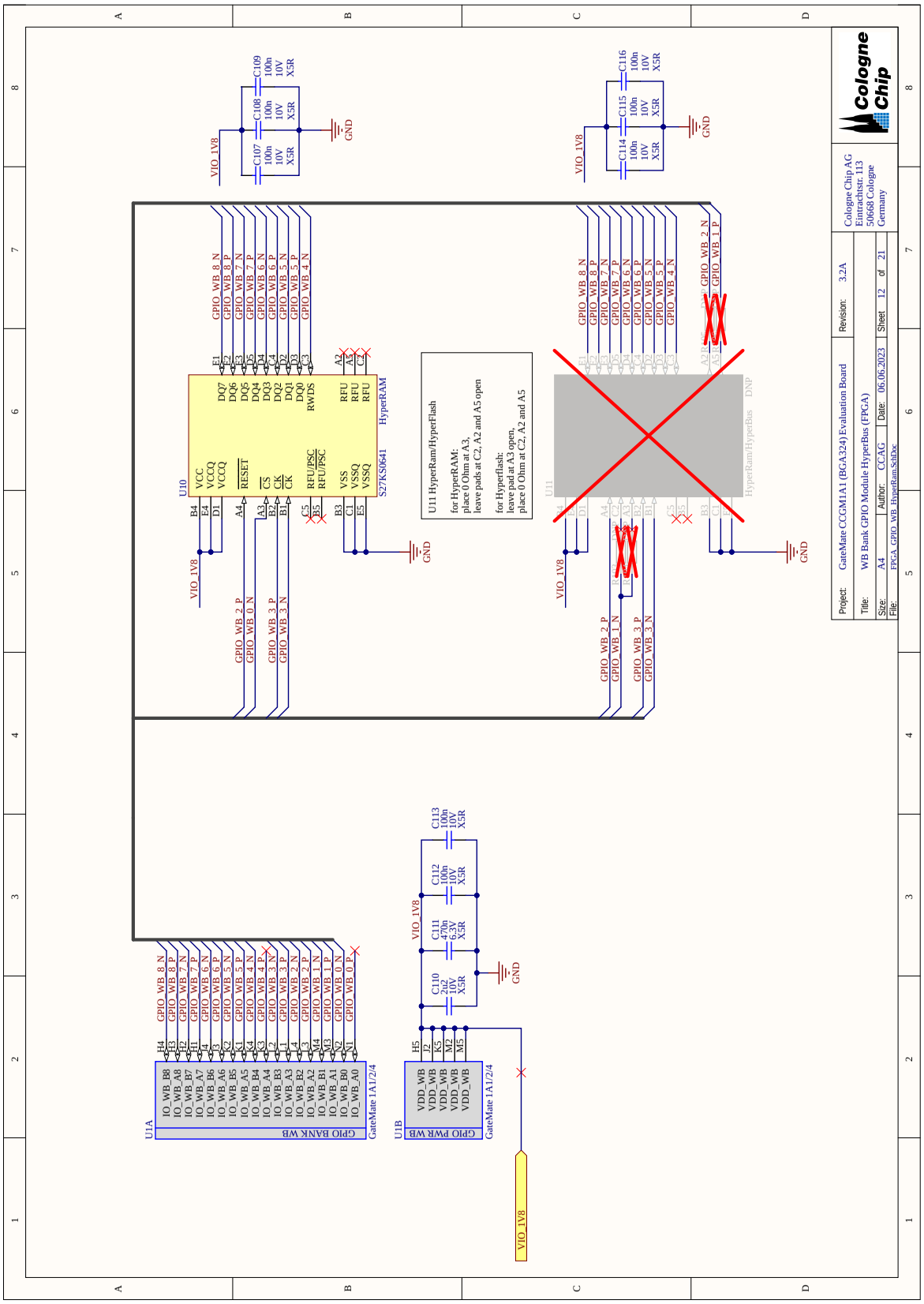
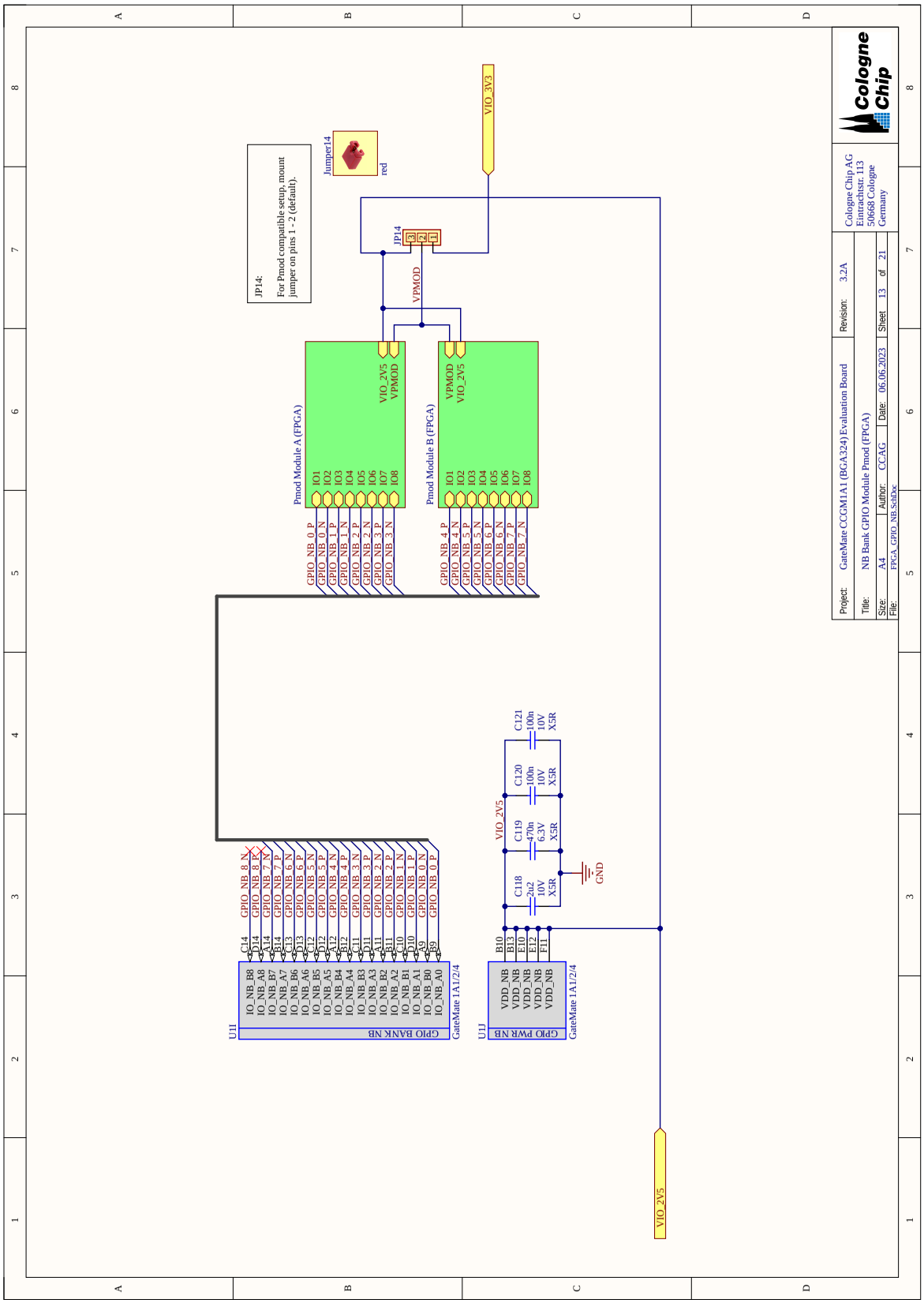
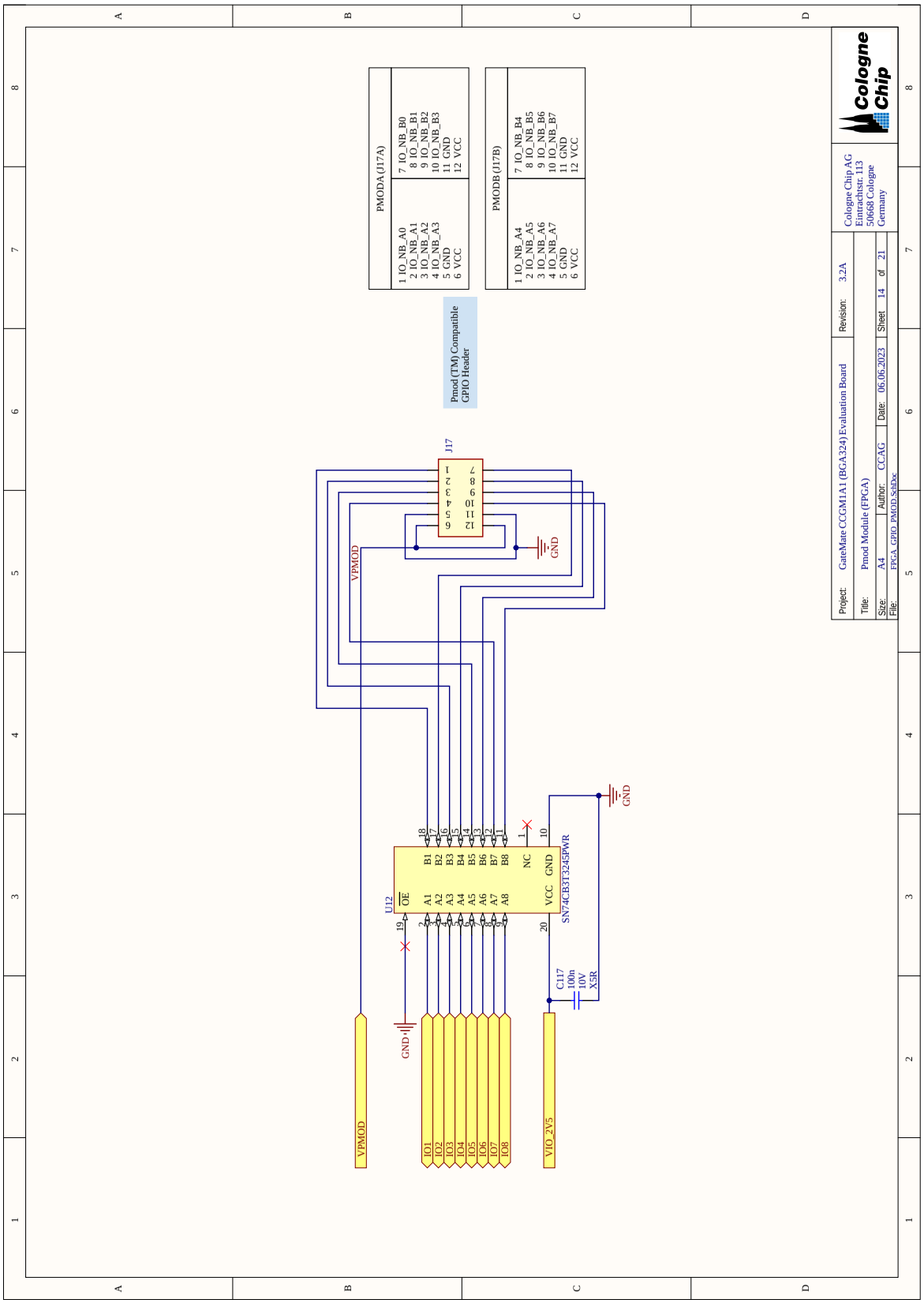
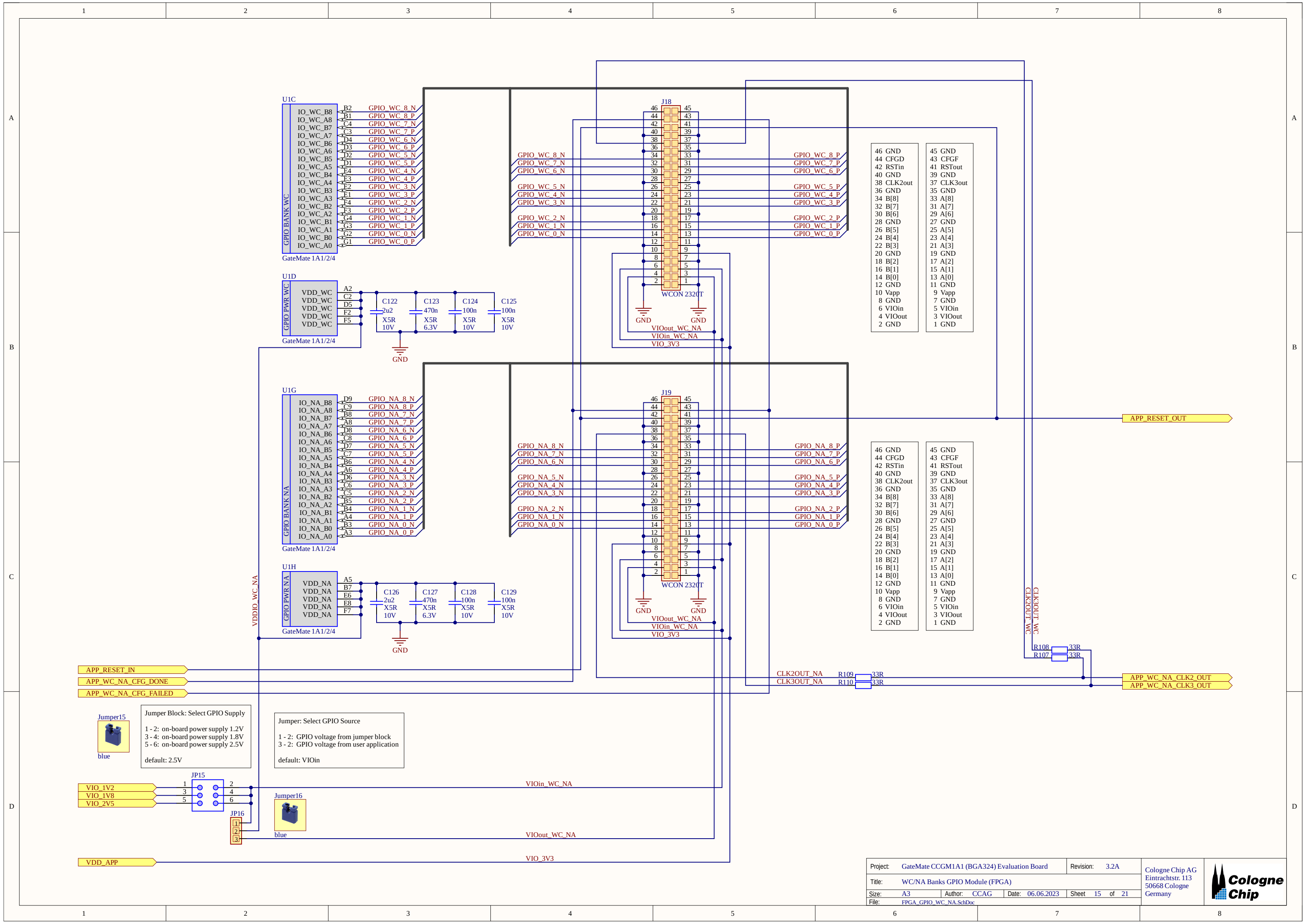
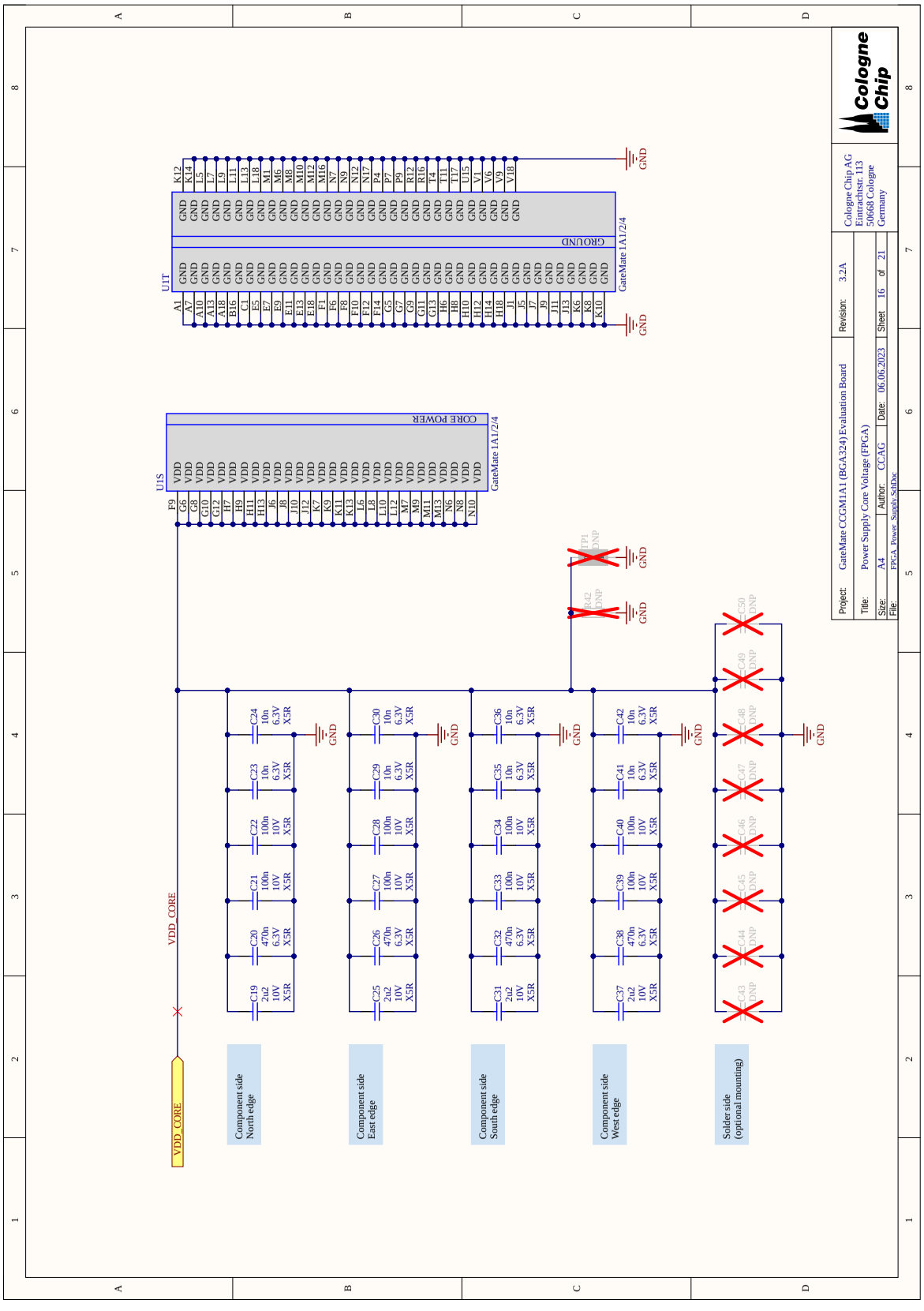
Germany


U10
S27KS0641
HyperRAM
U11 HyperRam/HyperFlash
for HyperRAM:
place 0 Ohm at A3,
leave pads at C2, A2 and A5 open
for Hyperflash:
leave pad at A3 open,
place 0 Ohm at C2, A2 and A5
U11
HyperRam/HyperBus
DNP
U1A
GateMate 1A1/2/4
GPIO BANK WB
U1B
GateMate 1A1/2/4
GPIO PWR WB
VIO_1V8
GND
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: WB Bank GPIO Module HyperBus (FPGA)
Size: A4
Author: CC:AG
Date: 06.06.2023
Sheet 12 of 21
File: FPGA_GPIO_WB_HyperRam.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


JP14:
For Pmod compatible setup, mount jumper on pins 1 - 2 (default).
Jumper14
red
VIO_3V3
JP14
VPMOD
Pmod Module A (FPGA)
Pmod Module B (FPGA)
VIO_2V5
VPMOD
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
GPIO_NB_0_P
GPIO_NB_0_N
GPIO_NB_1_P
GPIO_NB_1_N
GPIO_NB_2_P
GPIO_NB_2_N
GPIO_NB_3_P
GPIO_NB_3_N
GPIO_NB_4_P
GPIO_NB_4_N
GPIO_NB_5_P
GPIO_NB_5_N
GPIO_NB_6_P
GPIO_NB_6_N
GPIO_NB_7_P
GPIO_NB_7_N
GPIO_NB_8_N
U1I
GPIO BANK NB
GateMate 1A1/2/4
U1J
GPIO PWR NB
VDD_NB
C118
2n2
10V
X5R
C119
470n
6.3V
X5R
C120
100n
10V
X5R
C121
100n
10V
X5R
GND
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: NB Bank GPIO Module Pmod (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 13 of 21
File: FPGA_GPIO_NB.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


PMODA (J17A)
1 IO_NB_A0
2 IO_NB_A1
3 IO_NB_A2
4 GND
5 GND
6 VCC
7 IO_NB_B0
8 IO_NB_B1
9 IO_NB_B2
10 IO_NB_B3
11 GND
12 VCC
PMODB (J17B)
1 IO_NB_A4
2 IO_NB_A5
3 IO_NB_A6
4 IO_NB_A7
5 GND
6 VCC
7 IO_NB_B4
8 IO_NB_B5
9 IO_NB_B6
10 IO_NB_B7
11 GND
12 VCC
Pmod (TM) Compatible GPIO Header
J17
VPMOD
GND
U12
SN74CB3T3245PWR
VIO_2V5
C117
100n
10V
X5R
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Pmod Module (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 14 of 21
File: FPGA_GPIO_PMOD.Schdoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


Jumper Block: Select GPIO Supply
1 - 2: on-board power supply 1.2V
3 - 4: on-board power supply 1.8V
5 - 6: on-board power supply 2.5V
default: 2.5V
Jumper: Select GPIO Source
1 - 2: GPIO voltage from jumper block
3 - 2: GPIO voltage from user application
default: VIOin
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: WC/NA Banks GPIO Module (FPGA)
Size: A3
Author: CCAG
Date: 06.06.2023
Sheet 15 of 21
File: FPGA_GPIO_WC_NA.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


U1T
GateMate 1A1/2/4
GROUND
U1S
GateMate 1A1/2/4
CORE POWER
VDD_CORE
Component side North edge
Component side East edge
Component side South edge
Component side West edge
Solder side (optional mounting)
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Power Supply Core Voltage (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 16 of 21
File: FPGA_Power_Supply.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
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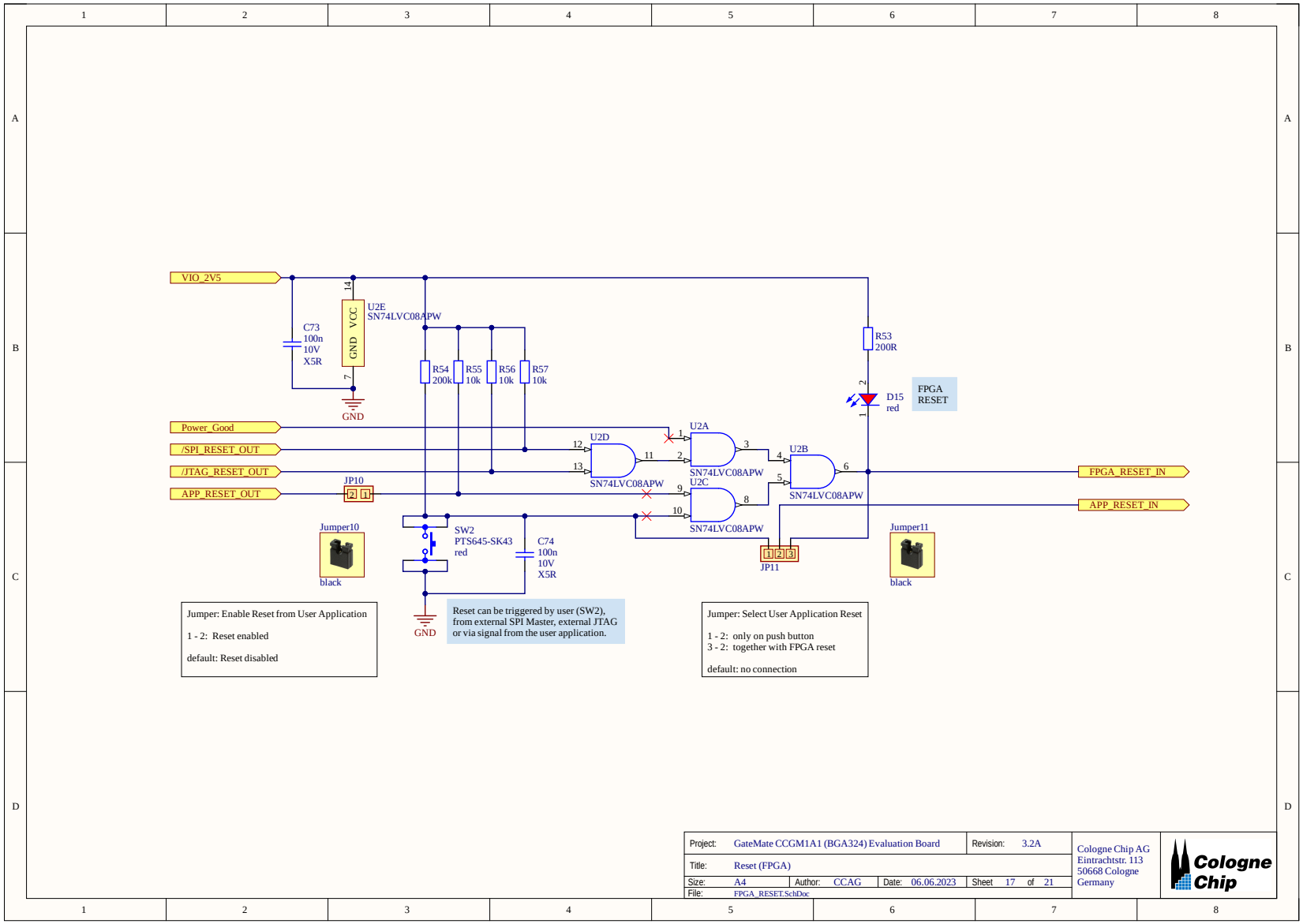
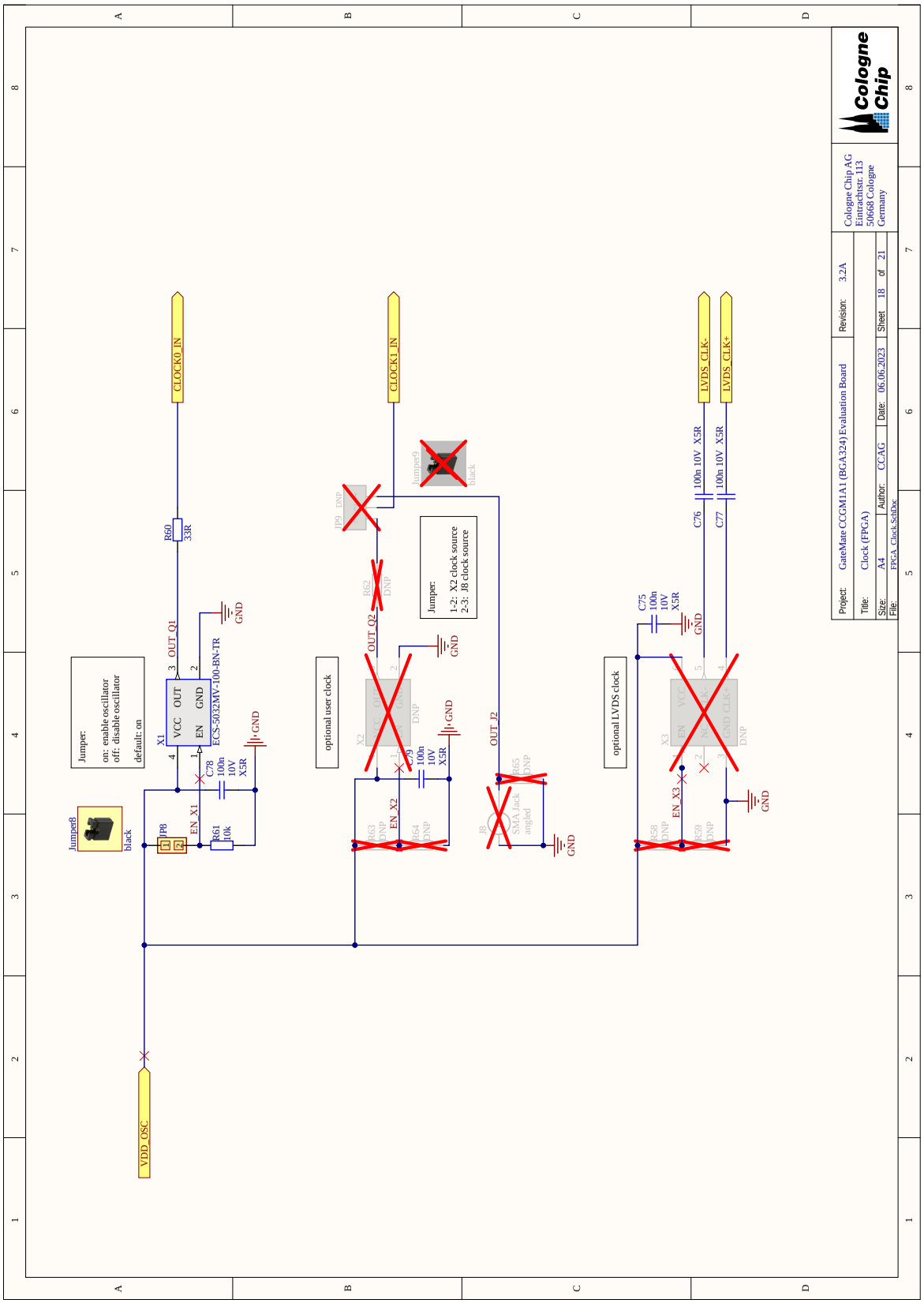
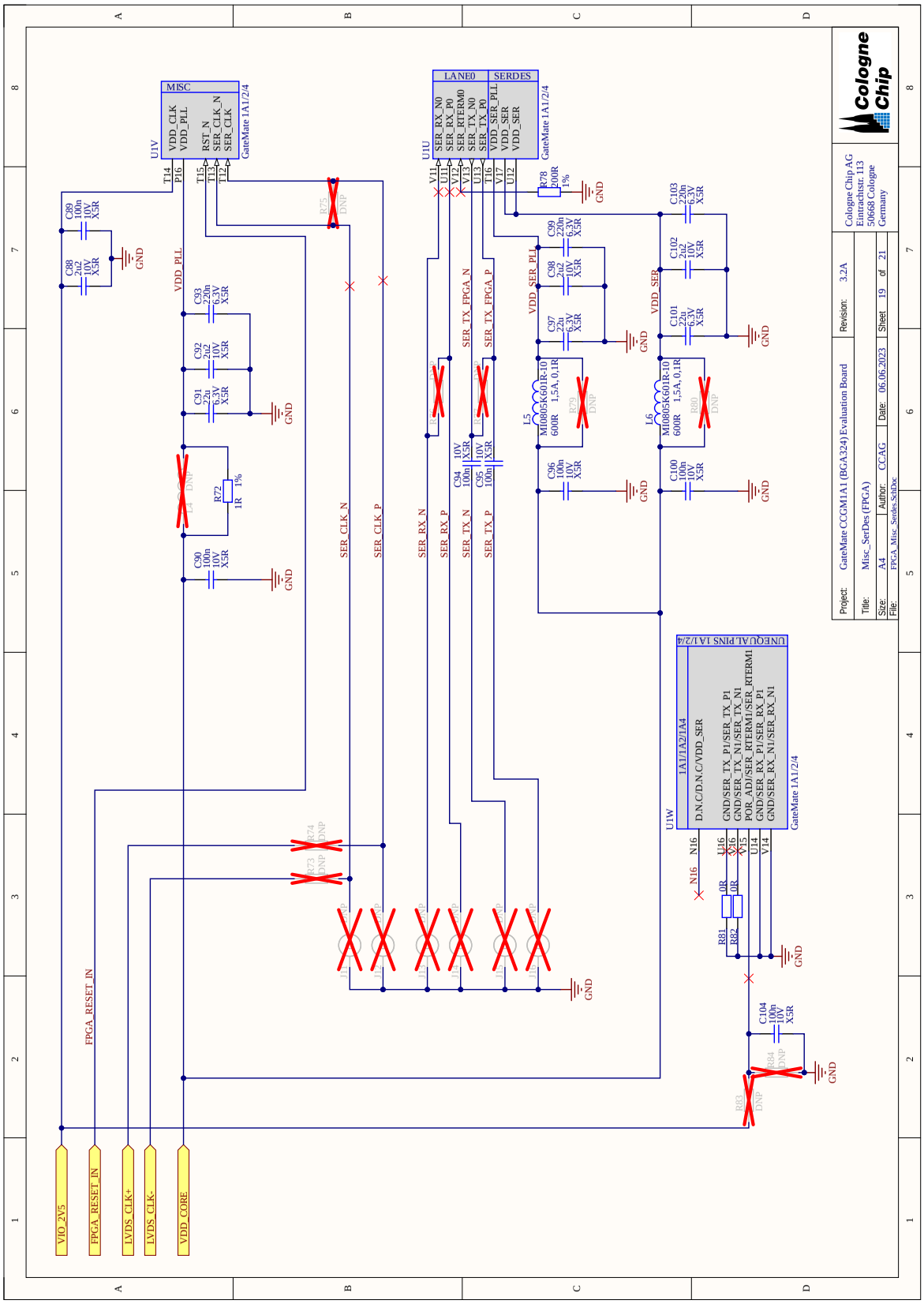
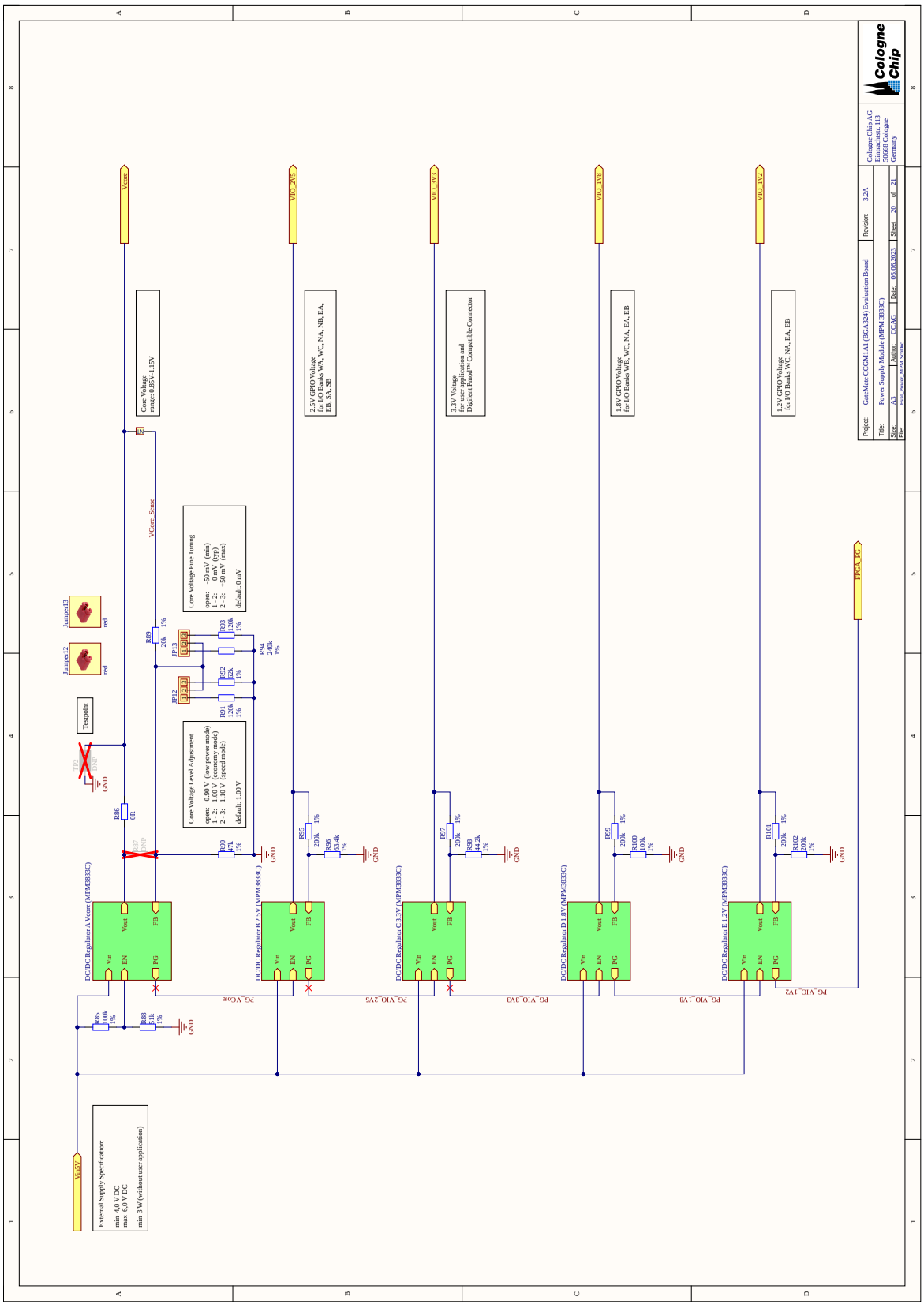
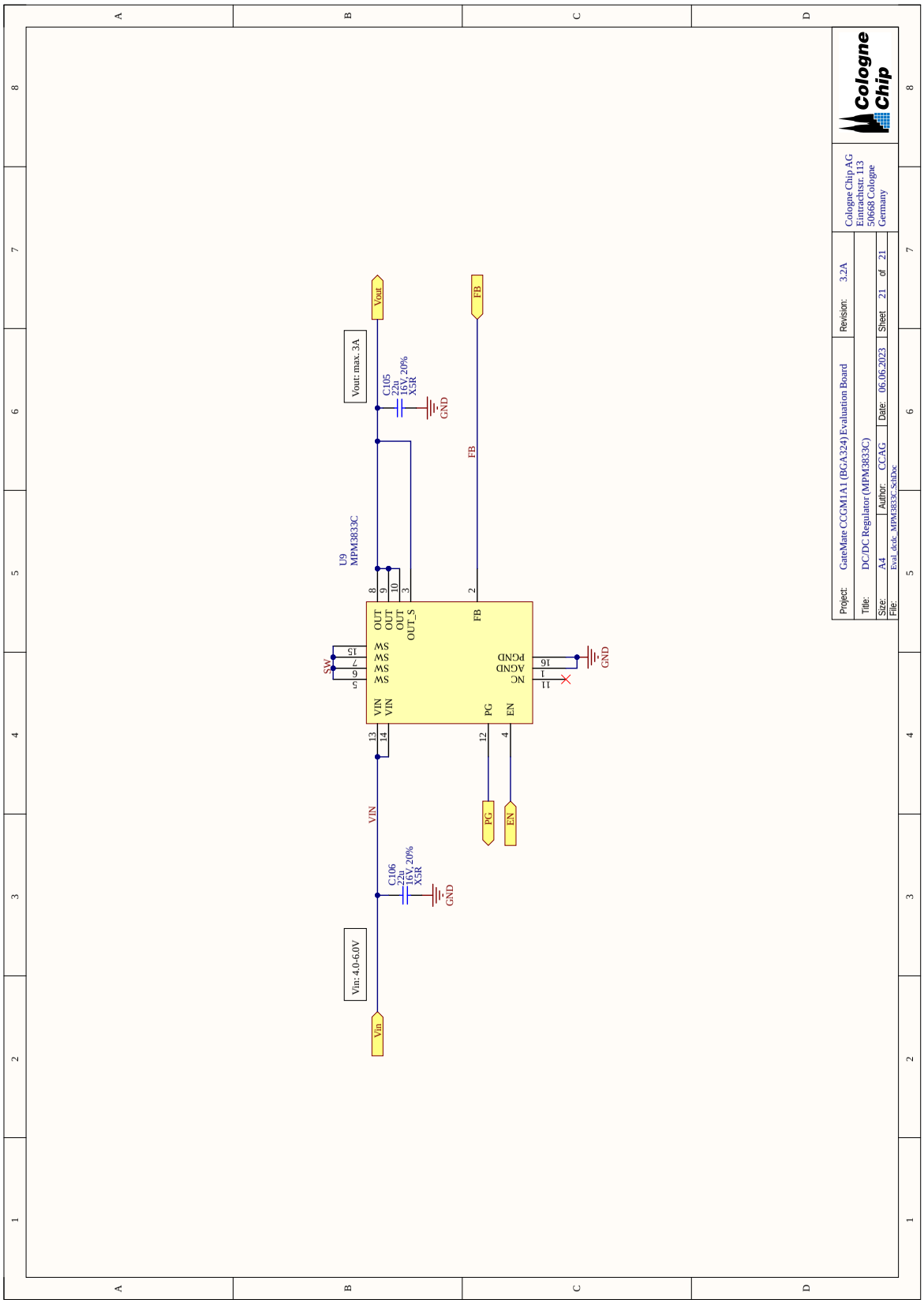

VIO_2V5
C73
100n
10V
X5R
U2E
SN74LVC08APW
GND
R54
200k
R55
10k
R56
10k
R57
10k
R53
200R
D15
red
FPGA
RESET
Power_Good
/SPI_RESET_OUT
/JTAG_RESET_OUT
APP_RESET_OUT
JP10
U2D
U2A
U2B
U2C
SN74LVC08APW
FPGA_RESET_IN
APP_RESET_IN
Jumper10
black
SW2
PTS645-SK43
red
C74
100n
10V
X5R
JP11
Jumper11
black
Jumper: Enable Reset from User Application
1 - 2: Reset enabled
default: Reset disabled
Reset can be triggered by user (SW2), from external SPI Master, external JTAG or via signal from the user application.
Jumper: Select User Application Reset
1 - 2: only on push button
3 - 2: together with FPGA reset
default: no connection
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Reset (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 17 of 21
File: FPGA_RESET.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Cologne Chip


CLOCK0_IN
CLOCK1_IN
LVDS_CLK-
LVDS_CLK+
VDD_OSC
OUT_Q1
OUT_Q2
OUT_J2
EN_X1
EN_X2
EN_X3
X1
X2
X3
ECS-5032MV-100-BN-TR
R60 33R
R61 10k
R62 DNP
R63 DNP
R64 DNP
R65 DNP
R58 DNP
R59 DNP
C78 100n 10V X5R
C79 100n 10V X5R
C75 100n 10V X5R
C76 100n 10V X5R
C77 100n 10V X5R
JP8
JP9 DNP
Jumper8 black
Jumper9 black
J8 SMA Jack angled
GND
Jumper:
on: enable oscillator
off: disable oscillator
default: on
optional user clock
Jumper:
1-2: X2 clock source
2-3: J8 clock source
optional LVDS clock
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Clock (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 18 of 21
File: FPGA_Clock.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


MISC
LANE0
SERDES
GateMate 1A1/2/4
VDD_PLL
VDD_SER_PLL
VDD_SER
SER_CLK_N
SER_CLK_P
SER_RX_N
SER_RX_P
SER_TX_N
SER_TX_P
SER_TX_FPGA_N
SER_TX_FPGA_P
FPGA_RESET_IN
VIO_2V5
LVDS_CLK+
LVDS_CLK-
VDD_CORE
GND
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: Misc_SerDes (FPGA)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 19 of 21
File: FPGA_Misc_SerDes.SchDoc


Vcore
VIO_2V5
VIO_3V3
VIO_1V8
VIO_1V2
Core Voltage
range: 0.85V-1.15V
2.5V GPIO Voltage
for IO Banks WA, WC, NA, NB, EA, EB, SA, SB
3.3V Voltage
for user application and
Digilent Pmod™ Compatible Connector
1.8V GPIO Voltage
for IO Banks WB, WC, NA, EA, EB
1.2V GPIO Voltage
for IO Banks WC, NA, EA, EB
VCore_Sense
Core Voltage Fine Tuning
Core Voltage Level Adjustment
Testpoint
Jumper13
Jumper12
red
FPGA_PG
VinSV
External Supply Specification:
min 4.0 V DC
max 4.6 V DC
min 3 W (without user application)
DC/DC Regulator A Vcore (MPM3833C)
DC/DC Regulator B 2.5V (MPM3833C)
DC/DC Regulator C 3.3V (MPM3833C)
DC/DC Regulator D 1.8V (MPM3833C)
DC/DC Regulator E 1.2V (MPM3833C)
PG_VCore
PG_VIO_2V5
PG_VIO_3V3
PG_VIO_1V8
PG_VIO_1V2
GND
Cologne Chip AG
Europa-Allee 13
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Title: Power Supply Module (MPM 3833C)
Size: A3
Author: CC AG
Date: 06.06.2023
Sheet 20 of 21
File: Eval_Power_MPM.schSch
Revision: 3.2A


Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.2A
Title: DC/DC Regulator (MPM3833C)
Size: A4
Author: CCAG
Date: 06.06.2023
Sheet 21 of 21
File: Eval_dcdc_MPM3833C.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Vout
Vout: max. 3A
C105
22u
16V, 20%
X5R
GND
FB
U9
MPM3833C
OUT
OUT
OUT
OUT_S
SW
SW
SW
SW
VIN
VIN
FB
NC
AGND
PGND
PG
EN
SW
GND
VIN
C106
22u
25V, 20%
X5R
Vin: 4.0-6.0V
Vin
PG
EN

Chapter 4

Bill of Materials

Table 4.1: *Bill of Materials (sorted by designator)*

Component	Specification	Designators	Count
10n	6.3V X5R	C18, C23, C24, C29, C30, C35, C36, C41, C42	9
4.7u	10V X5R	C54, C56, C63, C64, C65	5
8p	6.3V X5R	C67, C68	2
22u	6.3V X5R	C91, C97, C101	3
220n	6.3V X5R	C93, C99, C103	3
22u	16V, 20% X5R	C105A, C105B, C105C, C105D, C105E, C106A, C106B, C106C, C106D, C106E	10
2u2	10V X5R	C1, C5, C10, C16, C19, C25, C31, C37, C69, C71, C80, C84, C88, C92, C98, C102, C110, C118, C122, C126	20
470n	6.3V X5R	C2, C6, C11, C20, C26, C32, C38, C81, C85, C111, C119, C123, C127	13

Continued on next page

Table 4.0: *Bill of Materials (sorted by designator)*

Continued from previous page

Component	Specification	Designators	Count
100n	10V X5R	C3, C4, C7, C8, C9, C12, C13, C14, C15, C17, C21, C22, C27, C28, C33, C34, C39, C40, C51, C52, C53, C55, C57, C58, C59, C60, C61, C62, C66, C70, C72, C73, C74, C75, C76, C77, C78, C79, C82, C83, C86, C87, C89, C90, C94, C95, C96, C100, C104, C107, C108, C109, C112, C113, C114, C115, C116, C117A, C117B, C120, C121, C124, C125, C128, C129, C130, C131, C132	68
WE-150 060 VS7 322	LED green	D1, D2, D3, D4, D5, D6, D7, D8, D10	9
SP3012-04UTG	TVS diode	D14	1
WE-150 060 RS7 322	LED red	D9, D15	2
WE-150 060 YS7 322	LED yellow	D11, D12, D13, D16	4
WE-613 003 111 21	Header vertical 3 pins 2.54 mm	J6	1
WE-651 005 161 21	Mini USB 2.0 Type B Receptacle	J5, J7	2
WE-613 012 243 121	Socket header angled 2x6 pins 2.54 mm	J17A, J17B	2
WCON 2320T		J1, J2, J9, J10, J18, J19	6
WE-613 002 111 21	Jumper 2 pins	JP4, JP6, JP8, JP10	4
WE-613 006 211 21	Jumper 3x2 pins	JP3, JP15	2
WE-613 003 111 21	Jumper 3 pins	JP5, JP7, JP11, JP12, JP13, JP14, JP16	7
MI0805K601R-10	600R 1,5A, 0,1R	L1, L2, L3, L5, L6	5
WE-744 231 091	CNSW 370mA 90Ohm 100MHz	L7	1
BC847C		Q1, Q2	2
4k7	1%	R23, R24, R25, R29	4
2k	1%	R46	1
1k	1%	R43, R47, R48, R50	4
10k	1%	R19, R20, R21, R22, R26, R27, R31, R32, R33, R34, R35, R37, R51, R52, R55, R56, R57, R61	18
1R	1%	R72	1

Continued on next page

Table 4.0: *Bill of Materials (sorted by designator)*

Continued from previous page

Component	Specification	Designators	Count
0R	1%	R66, R70, R71, R81, R82, R86	6
51k	1%	R88	1
20k	1%	R89	1
47k	1%	R90	1
62k	1%	R92	1
120k	1%	R91, R93	2
240k	1%	R94	1
63.4k	1%	R96	1
44.2k	1%	R98	1
100k	1%	R85, R100	2
200k	1%	R14, R54, R95, R97, R99, R101, R102	7
33R	1%	R1, R2, R3, R4, R13, R15, R16, R17, R18, R38, R39, R40, R41, R60, R107, R108, R109, R110	18
12k	1%	R44, R45, R49, R111, R112, R113, R114, R115	8
200R	1%	R5, R6, R7, R8, R9, R10, R11, R12, R28, R30, R53, R78, R116	13
219-4MSTR	DIP switch 4 positions	SW1	1
PTS645-SK43	push button red	SW2	1
PTS645-SL43	push button black	SW3	1
CCGM1A1	GateMate FPGA	U1	1
SN74LVC08APW		U2	1
SN74LVC1G34DBVR		U4	1
MX25R6435F	64 MBit	U5	1
MIC5504-3.3YMT-TZ		U6	1
FT2232HQ-Reel		U7	1
93LC56BT-I/OT		U8	1
MPM3833C		U9A, U9B, U9C, U9D, U9E	5
S27KS0641		U10	1
SN74CB3T3245PWR		U12A, U12B, U13, U14	4
SN74AUC00RGYR		U15	1
SN74AUP1G04DRYR		U16	1
ECS-5032MV-100-BN-TR	10 MHz	X1	1
7M-12.000MAHV-T		X4	1

GateMate™ FPGA
Evaluation Board Datasheet
Evaluation Board Version 3.2 / CCGM1A1
Schematics
DS1003
January 2024

Cologne Chip